

A New Undergraduate Semiconductor Manufacturing Option in the Chemical Engineering Curriculum

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The engineering curriculum reform in the 21st century should focus on providing students with a broad knowledge base and crosscutting programs in interdisciplinary fields including semiconductor manufacturing and nanotechnology. The traditional engineering education training is often inadequate in preparing the students for the challenges presented by this industry's dynamic environment, and insufficient to meet the employer's criteria in hiring new engineers. This paper describes a new multidisciplinary curriculum and training program at UCLA. The program provides knowledge and skills in semiconductor manufacturing through a series of courses that emphasize on the application of fundamental engineering disciplines in solid-state physics, materials science of semiconductors, and chemical processing. This new curriculum was recently accredited by the Accreditation Board for Engineering and Technology (ABET).

INTRODUCTION

THE MICROELECTRONICS INDUSTRY has evolved significantly since the invention of the 1st solid-state transistor by Bardeen, Brattain, and Shockley at Bell Labs in 1947. The advances in microelectronics technology have revolutionized the telecommunication industry; and this has greatly changed the way people and nations interact and the way that they exchange information.

The heart of this industry is the computer chip and the tiny solid-state electronic devices that it comprises. By constantly shrinking the device dimensions, ultra-large scale integrated circuits (ULSI) have become increasingly powerful, while the cost per function has continued to decrease. For example, memory cells at dimensions below 130 nanometers can store gigabits of information in computers, and quantum electronic devices made from compound semiconductors can provide signal switching and amplification at speeds in excess of 150 gigahertz. These technological advances become possible with the use of sophisticated chemical processes for depositing, patterning, and etching thin-film circuits onto semiconductor surfaces.

It is possible to categorize the microelectronics industry into three major components:

1. Equipment and material manufacturing that enables the fabrication of IC's.
2. Semiconductor device fabrication that provides the building blocks of commercially viable equipment.

3. Electronic equipment such as digital camera, cellular phones, and direct TV.

All three industries rely heavily on semiconductor manufacturing; thus, along with microprocessor design and communication, Intel has clearly identified semiconductor manufacturing as one of the three key elements to its company. It is obvious that semiconductor manufacturing is one of the most critical components in further advancing the technology.

Chemical Engineering is a discipline with a broad science and technology base, and its practice has led to numerous technological innovations in energy, environment, medicine, biotechnology, and most recently, microelectronics. Chemical engineers have an important role to play in semiconductor manufacturing, in design, operation and control of the sophisticated chemical processes that fabricate the chips. They also maintain continuous involvement in research and development of new processes that are capable of making the next generation of denser and denser integrated circuits. These engineers require a knowledge of mathematics, physics and chemistry that is appropriate when working with engineering materials having dimensions between 10 and 1000 angstroms.

To maintain the rate of progress of innovations and inventions, there is an unprecedented demand for highly educated and trained engineers in the semiconductor manufacturing industry both in the United States, and throughout the world. The demand for experienced engineers is at all degree levels and has intensified with the development of revolutionary new products for the internet, computers, and for communication technologies. Since Engineering Education is career oriented

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[1, 2], there is a need for curriculum reform to meet the dynamic changes in employment, starting at the undergraduate degree level.

Engineers with at least a four-year college degree account for one-third of the workers in this industry, and there is an ever increasing demand from government laboratories, industries, and academia for students with specialized training in semiconductor manufacturing. However, the traditional engineering education training is often inadequate in preparing the students for the challenges presented by this industry's dynamic environment, and insufficient to meet the employer's criteria in hiring new engineers.

Clearly, the University should provide the additional resources necessary to change the teaching methods used for education in materials engineering. It is critically important to train the students in the various scientific and technological areas that are pertinent to microelectronics and nano-fabrication industries, and allow them to practice engineering principles in a laboratory environment with state-of-the-art experimental setup. It is usual to offer specialty laboratory courses on microelectronics fabrication in Electrical Engineering departments throughout the country. Consequently, students only get training in this area through courses co-listed [3] in chemical engineering departments, or some specialty courses such as thin film processing [4] but with no chemical engineering facilities. This limits the exposure of chemical engineering students to additional courses that would further enhance their knowledge base. Recently, laboratory courses with emphasis on semiconductor manufacturing have been introduced into the Chemical Engineering Curricula:

- The Department of Chemical Engineering at Oregon State University included plasma etching and spin coating in the Unit Operations laboratory and teaches a course on Chemical Process Statistics as a part of an option in "Microelectronics Processing" [5].
- The Department of Chemical Engineering at the University of Illinois, (Chicago), addressed this concern by using the world-wide web to instruct a course on microelectronics processing [6, 7] and provide students with flexible working hours and schedules.
- The Department of Chemical and Material Engineering at the San Jose State University set up a new concentration in Microelectronics Process Engineering [8] to address this issue. They require Chemical Engineering students to take a prerequisite course before starting the laboratory course that focuses on cooperation learning.
- The Department of Chemical Engineering at Colorado School of Mines also has a similar course on Interdisciplinary Microelectronics Processing Laboratory [9]. They require stu-

dents to take a prerequisite course before starting the laboratory course.

This paper presents a new multidisciplinary curriculum and training program to provide a systematic education for Chemical Engineering students in Semiconductor Manufacturing and Nanotechnology. Provision of knowledge and skills occurs through a series of six courses that emphasize the application of fundamental chemical engineering disciplines in solid-state physics, materials science of semiconductors, and chemical process engineering. The curriculum has three major components:

1. A comprehensive curriculum in semiconductor manufacturing.
2. One laboratory for hands-on training in semiconductor device fabrication.
3. An interactive website learning format that provides access to students outside UCLA and industrial mentors.

The curriculum contains specialty courses on various technologies used to fabricate microelectronics devices, including, for example, chemical vapor deposition, plasma processing, photolithography, wet-chemical cleaning, ion implantation, silicon oxidation, and contamination control. The instruction culminates in the laboratory course: Semiconductor Processing Laboratory [10]. The laboratory hours provide students with hands-on training on IC fabrication, and give them an opportunity to investigate new manufacturing technologies. Moreover, the posting of course materials and lab experiments on the website will allow interactive learning outside the classroom.

CURRICULUM DEVELOPMENT

The Chemical Engineering Department at UCLA offers a wide selection of undergraduate courses and five options:

- General chemical engineering
- Semiconductor manufacturing
- Environmental engineering
- Bioengineering
- Biomedical engineering.

Many undergraduate students also take advantage of numerous graduate-level subjects and research topics in their senior years. This type of exposure is invaluable in preparing them for work as chemical engineers for graduate school, industry, or government in chemical engineering.

The Department of Chemical Engineering at UCLA offers students a comprehensive curriculum in solid-state physics, materials characterization, semiconductor processing, and the principles of IC manufacturing. The new semiconductor manufacturing option is designed to provide in-depth knowledge of the field such as Surface and Interface Engineering, Electrochemical Processing, Plasma Processing of Materials, and Physical and

Table 1. Semiconductor manufacturing option.

	FALL	WINTER	SPRING
1st YEAR	(4) Chemical Structures (4) Calculus & Anal. Geom. (5) English Composition	(4) Chem Energetics and Change (4) Calculus & Anal. Geom. (5) Physics for Scientists and Engineers (4) Gen Elective*	(2) Gen Chem Lab (4) Intro Organic Chem (4) Calculus/Several Variables (7) Physics for Scientists and Engineers & Lab
2nd YEAR	(4) Intro Chem Eng (3) Gen Chem Lab (4) Calculus/Several Variables (7) Physics for Scientists and Engineers & Lab	(4) Intro Eng Thermo (6) Organic Chem (4) Linear Algebra and Applications (4) Intro to Computing	(4) Intermediate Inorganic Chem (4) Infinite Series (4) <i>Science of Engineering Materials</i> (4) Gen Elective
3rd YEAR	(4) Momentum transfer (4) Math in Chem Eng (4) Physical Chem (4) Electrical and Electronic Circuits	(4) Heat Transfer (4) Chem Eng Thermo (4) <i>Physics of Materials</i> (4) Gen Elective	(4) Mass Transfer (4) Separation Process (6) Chem Eng Lab I (4) Gen Elective
4th YEAR	(4) <i>Physical Principles of Semiconductor Devices</i> (4) Chem Reaction Eng (4) Chem Elective (4) Gen Elective	(6) <i>Semicond. Manf. Lab</i> (4) Proc Dynamics and Control (4) Proc Economics and Analysis (4) <i>Semicond. Manf. Elective</i>	(4) Chem Proc Computer-Aided Design and Analysis (4) <i>Semicond. Manf. Elective</i> (4) Chem Elective (4) Gen Elective

The numbers in parenthesis represent the credit units, and the courses shown in italic bold fonts are courses specific to this semiconductor manufacturing option.

*General Elective

Chemical Vapor Deposition. The curriculum is similar to the core curriculum, with only a number of changes, as shown in Table 1:

- Reduce the advanced chemistry electives from three to two.
- Add the Science of Engineering Materials course (MSE 14) to replace one chemistry elective.
- Add the Physics of Materials course (MSE 120) to replace the Introduction to Mechanics of Deformable Solids course (C&EE 108).
- Add the Physical Principles of Semiconductor Devices course (EE2).
- Replace one undergraduate unit operation laboratory course with the newly established semiconductor manufacturing laboratory course.
- Require two elective courses in semiconductor manufacturing.

Core course requirements

Students majoring in the Semiconductor Manu-

Table 2. Course requirement in the Semiconductor Manufacturing Option

Course Requirements (47 courses, 199 units)	
Chemical Engineering	14 courses
Chemistry & Biochemistry	8 courses
Mathematics	6 courses
Physics	3 courses
Material Science & Engineering	2 courses
Electrical Engineering	2 courses
Computer programming	1 course
English	1 course
Elective courses	
— General Education	6 courses
— Semiconductor Manufacturing	2 courses
— Chemistry	2 courses

facturing Option start to take specialty courses as early as the last quarter in their sophomore year. Table 2 shows the course requirement in various disciplines.

- *Science of Engineering Materials*: this course introduces the students to various materials used in engineering design
- *Physics of Materials*: this course teaches students the electronic, optical, and magnetic properties of solid materials
- *Physical Principles of Semiconductor Devices*: this course prepares students on the fundamentals of semiconductor materials, p-n junctions, and semiconductor based electronic devices.

These prerequisite courses prepare the students for the capstone laboratory course on Semiconductor Manufacturing, the detail of which follows later.

Specialty course requirements

Besides the core courses, two elective courses in the semiconductor manufacturing area are required from the course listing below.

1. Fundamental Subjects:
 - Physics of Semiconductor Devices
 - Materials Science of Semiconductors
 - Chemical Process Science
 - Mechanical Design and Robotics
 - Semiconductor Equipment Laboratory
 - Semiconductor Device Processing Laboratory
2. Advanced Topics:
 - Principles of ULSI Fabrication Processes
 - Semiconductor Surface Science
 - Chemical Vapor Deposition
 - Reaction Kinetics of Semiconductor Processes

- Principles in Plasma Processing
- Semiconductor Process Simulation and Modeling
- Electronic Packaging and Interconnection
- Flat Panel Display Technologies

The UCLA School of Engineering is world renowned for its scholarship in semiconductor physics, chemistry and engineering, through its multidisciplinary approach towards the education and training for our undergraduate students. In addition, prominent semiconductor companies sponsor student research and training, and there are ample opportunities for interaction with the sponsors, including industry internships.

SEMICONDUCTOR MANUFACTURING LABORATORY DEVELOPMENT

This new course is a six credit unit course that comprises of four hours of lectures and four laboratory hours each week to provide both knowledge and training in semiconductor manufacturing. Organization of the lectures is modular, as detailed below. In the laboratory, students form

teams with electrical engineers and material scientists, then carry out the entire process flow for making solid state devices, including capacitors, p-n junctions, and complementary metal-oxide-semiconductor (CMOS) transistors. Students are required to synthesize and apply the knowledge they learned to the engineering of semiconductor manufacturing processes.

Course outline

- Introduction to Solid State Device Fabrication
- Optical Lithography
- Crystal Growth
- Oxidation
- Wafer Cleaning and Diffusion
- Ion Implantation
- Film Deposition (semiconductors, dielectrics, and metals)
- PN Junction and MOS Devices
- MOSFET and Electrical Characterization
- Film Patterning (etching)
- Metallization (interconnection)
- Design of Experiments

In the first seven weeks of the quarter, the course focuses on theory and models for various chemical processes. In the last three weeks, the course focuses on electronic device characterization.

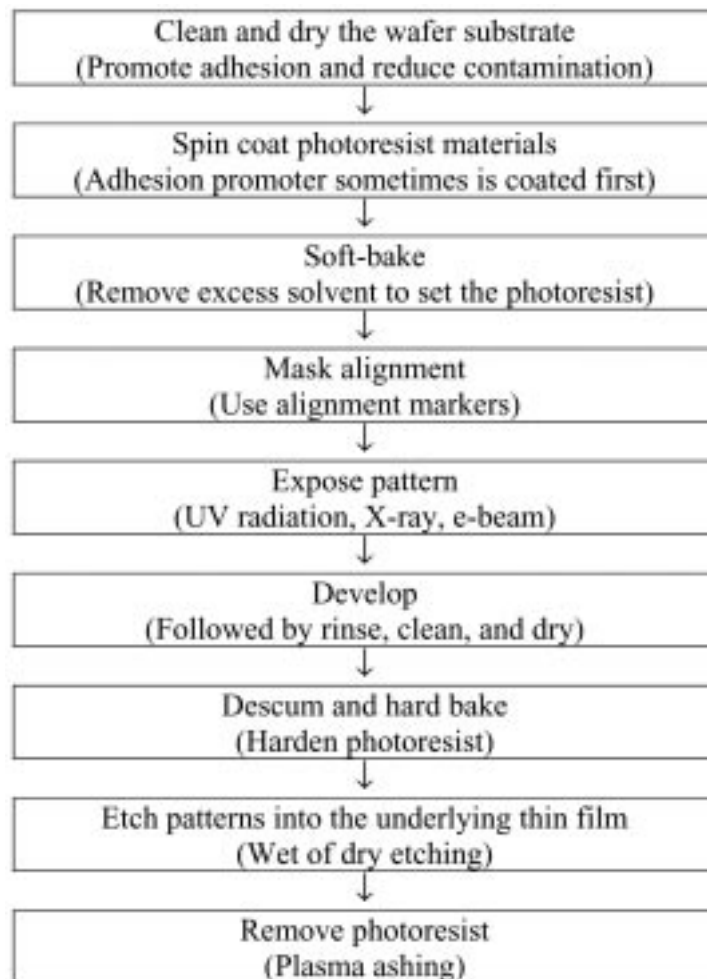


Fig. 1. Photolithographic process flow.

Lectures

Each course module focuses on either a unit operation of the chemical processes, theory of electronic devices, or device testing. Briefing of two course modules and a sample of students' homework occur here [11].

a) *Photolithography Process*. This course module systematically explains the photolithographic processes used in the microelectronic industry, as shown in Fig. 1.

The topics included are:

- masks design and type,
- various exposure light source such as mercury arc lamp, X-ray, electron beam, and
- ion beam for defining micrometer to nanometer scale features.

Various exposure techniques are discussed in the class, including contact printing, proximity printing, and projection printing. An example is a commonly used step-and-repeat projection system [12], illustrating the patterning of well-defined features onto a die of silicon and an entire silicon wafer. Detailed discussion on photo-sensitive resist materials provides students with a deep understanding of the versatility of the process. Starting with the spin-on process, examination of Novolac based positive and negative photoresist involves details such as contrast and sensitivity.

The course additionally details the use of chemical amplification for patterning finer features in deep-UV photoresist, using adhesion promoters and anti-reflective coating (ARC) for enhanced process performance. Discussions on optics include:

- diffraction
- coherence
- numerical aperture (NA)
- depth of focus
- modulation transfer function.

Examples include the practical implications of a few photoresist processing steps such as plasma descum and photoresist reflow.

b) *Ion Implantation Process*

Ion implantation is one important process step in microelectronics fabrication. Ion implantation is an alternative to diffusion for introducing known concentrations of dopants into specific locations in silicon wafers. During the ion implantation process, energetic ions penetrate a solid target, lose their energy due to collisions with atomic nuclei and electrons in the target solid, and eventually come to rest.

The range, (R) is the total distance that ions travel in the target before they stop. The range is often not a straight line due to the interactions between the ions and the solid, and the projected range (R_p) is the projection of this range. Moreover, not all ions with the same energy stop at R_p .

There is also a statistical fluctuation along the direction of the projected range called the projected or normal straggle, (ΔR_p). Scattering also occurs in the direction perpendicular to the ion trajectory, and the statistical fluctuation along this direction is termed the projected lateral straggle or transverse straggle, ΔR_{\perp} .

The theory of ion stopping including nuclear stopping and electronic stopping is discussed with the Lindhart, Scharff, and Schiott (LSS) model, a mathematical formula that describes the concentration distribution of the implanted ions in amorphous materials as a Gaussian distribution:

$$C(x) = C(R_p) \exp\left(-\frac{(x - R_p)^2}{2\Delta R_p^2}\right)$$

The overall dose (atoms/cm²) is:

$$Q = \int_{-\infty}^{\infty} C(x) dx = \sqrt{2\pi} C(R_p) \Delta R_p$$

Therefore, the peak concentration of the dopant at R_p is:

$$C(R_p) = \frac{Q}{\sqrt{2\pi} \Delta R_p} \cong \frac{0.4Q}{\Delta R_p}$$

The LLS model assumes implantation occurs in amorphous materials can be approximated by a Gaussian distribution. This is not completely correct, but in many cases is a good first order description.

The lectures also detail other important issues in ion implantation [13], including:

- implanting into single crystal: channeling;
- implantation damage;
- dopant activation annealing;
- selecting mask layer and thickness;
- Monte Carlo simulation of an implanted profile (TRIM).

Sample of student homework

Students training includes the use of Monte Carlo based software (TRIM) that allows the students to learn the dynamics during ion implantation process. This topic ties very nicely to the mass-transfer problems in dopant diffusion that the students also learned in the class. Figure 2 shows an example of students' homework simulation results on ion distribution.

TRIM is an experimental and research software ('The Stopping and Range of Ions in Solids', IBM software (1985) ISBN-0-08-021603-X) developed by IBM for non-commercial and experimental use by researchers and students. Ion implantation is simulated by using Monte Carlo simulation to track the history of an ion through successive collisions with target atoms, using the binary collision assumption detailed above. This determines the trajectory of each ion as a function of its energy, position, and direction, while calculations

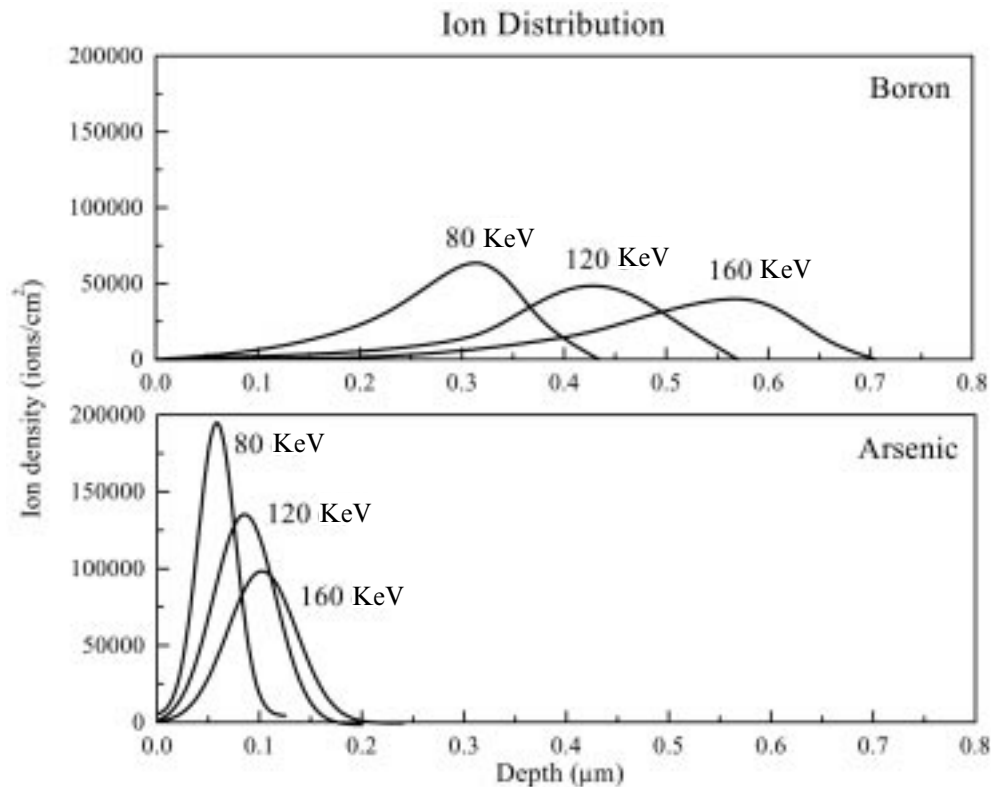


Fig. 2. Ion implantation simulation.

involving a large number of ion trajectories yield statistically meaningful results.

CMOS fabrication in the micro-fabrication laboratory

Inside the Nanoelectronics Research Facility [14] at UCLA there is a dedicated student micro-fabrication laboratory, $\sim 700 \text{ ft}^2$. This is a class 1000 HEPA filtered clean room where students conduct photolithography, wet cleaning, wet etching, and all metrology measurements. The Nanoelectronic Research lab is also available for advanced material processing steps. The list shown below details the equipment available for the undergraduate teaching laboratory:

a) Lithography tools

- Quintel 2001 contact aligner
- Photoresist coater and developer
- Baking station.

b) Wet processing tools

- Wet chemical cleaning bench for RCA and HF cleans
- Spin-rinse dryers
- Wet chemical etching bench for dielectrics and Al patterning.

c) Metrology tools

- Nanospec AFT
- Gaertner L116B automatic ellipsometer with variable angle of incidence
- Tencor Alpha Step 200 profilometer

- Omnimap 4 point probe for mapping sheet resistances
- HP probe stations for I-V measurements.

d) Thermal processing tools

- Thermal oxidation and annealing furnace
- Metal sintering furnace.

e) Thin film processing tools

- Low pressure chemical vapor deposition furnace
- Three-target metal sputtering deposition system
- Plasma enhanced chemical vapor deposition
- Reactive ion etcher.

The laboratory is currently capable of training 20 students per quarter. Students learn how to use state-of-the-art equipment to fabricate solid-state electronic devices and characterize the electronic device performance, as shown in Figure 3.

A list of the detailed process flow for CMOS fabrication appears in Table 3, with cross-sectional views of the CMOS devices after various implantation processes, and the fully processed device. Also included at the end of the table are two representative electrical characterizations of the MOSFET transistors and inverters.

Figure 4 shows an SEM image of devices fabricated by the students. Each team has to turn in a comprehensive team report at the end of the quarter summarizing the processing details and electrical characterization.



Fig. 3. Lecturing and device testing in the laboratory course: (a) students testing microelectronic devices; (b) lecturing in the micro-fabrication lab.

Student laboratory report

The laboratory report is an integral component of the student overall performance in the class. Starting with an executive summary, students include an introduction, a concise summary and discussion of their fabrication process and experimental results including process measurements and device measurement.

Using the theory of the fabrication processes from the lectures, students predict process parameters such as:

- field oxide thickness and color
- gate oxide thickness
- junction depths and doping levels
- sheet resistances
- polysilicon thickness
- aluminum thickness and sheet resistance.

They also make comparisons with actual measurement when possible. The device parameters include measurements from:

- diode
 - a) saturation current
 - b) forward turn-on voltage
 - c) reverse breakdown voltage
 - d) ideality factor.
- MOSFET
 - e) threshold voltage

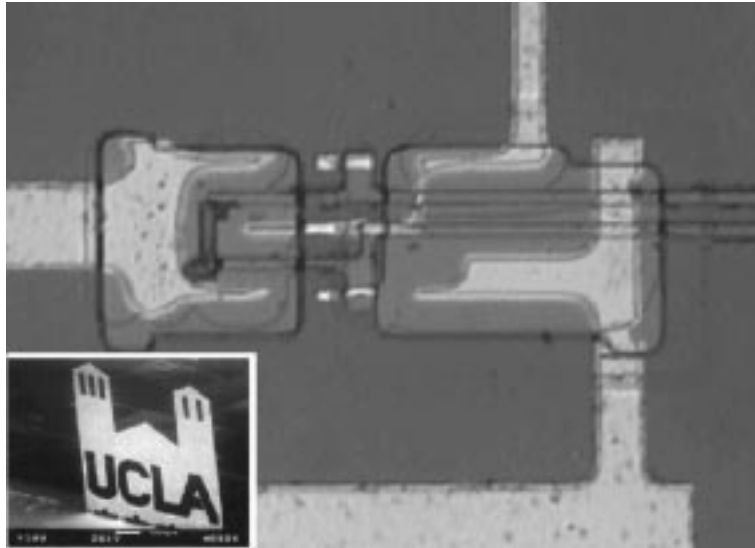


Fig. 4. CMOS (MEMS) device fabricated at UCLA.

- f) transconductance
- g) channel mobility
- other devices such as bipolar junction transistor and ring oscillator.

The most important part of the report is the discussion. Students have to provide a thorough evaluation of the experimental results and explanation for any discrepancies between the measurements and calculations and suggest modifications to the processes to improve the device performance when applicable. They are graded on the insight show in correlating device characterization to process sequences since this is the most critical part of their training.

ASSESSMENT

In its first offering in the Spring quarter of 2000, the semiconductor manufacturing laboratory course attracted the maximum number of students (15 students) that the facility could safely accommodate. The students appraised the course and the instructor with an excellent overall rating of 8.42/9.00. The students are very positive about their learning experience and some of their comments include:

- The material covered a broad range of topics related to the objective of the course.
- The instructor is masterful in objectives.
- The lecture notes were very helpful and well organized.
- We wish to do more practical work in the lab sessions.

As the ultimate measure of the success of this option is the placement of our students after they

graduate, we are pleased to see that students who completed this option successfully have entered the workforce in the semiconductor industry. Many sent back their acknowledgments on the value of the course after they started working:




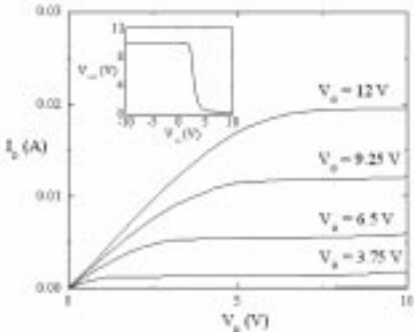
Message from one student at TRW: The course that you put together allowed me to pick up the manufacturing process at TRW within weeks. Even though I am working with GaAs and InP HBT, the basic processing is still the same as 104c. I am currently working in the lithography area. I [am] responsible for mostly making sure the Ultra Tech Steppers are running smoothly; if something goes wrong I have to run experiments to figure out what's wrong.

Message from one student at Novellus: Our group is focusing on tungsten CVD, so the main tool is for tungsten deposition. Although the tool is more advance than what I learned in 104C class, the concept of the whole process are similar. I would say 104C lectures are very useful, because the lectures really assist me in quick and better understanding of the process methodology. In addition, it's wonderful that you showed us Integra One in 104C class and explained about the loadlock system. In the fabs, I saw loadlock systems everywhere, and they remind me your last lecture in the nanolab.

As a result of students' positive feedback, together with the high level of interest in this option expressed by a large number of students, renovations over the summer of 2000 have made it possible to increase the number to 20 students per quarter. The lab course will be offered twice a year to accommodate the large number of students interested in majoring in this option (up to 40 students a year).

A feature about this option also appeared in an article titled 'Learn to Make Your Own Semiconductor Device' in the NSF Engineering On-Line News [15]:

Table 3. CMOS device fabrication process flow.

Process Flow	
<p>Week 0</p> <ol style="list-style-type: none"> 1. Wafer cleaning and inspection 2. Field oxide growth at 1000°C, wet, 800nm 3. Mask #1 + Lithography: define N-well 4. Oxide etch 5. Photoresist removal (plasma ashing, descum, and piranha etch) 6. N-well ion implantation (phosphorous) 7. Field oxide growth at 1000°C, 800nm 8. N-well annealing: N₂, 1050°C, 5 hours  <p>Device cross-section after N-well implantation</p> <p>Week 1</p> <ol style="list-style-type: none"> 1. Mask #2 + Lithography: define active area 2. Oxide etch 3. Photoresist removal <p>Week 2</p> <ol style="list-style-type: none"> 1. Wafer cleaning 2. Gate oxidation: 1050°C, dry, 60nm 3. Polysilicon deposition (LPCVD): 600°C, 400nm 4. Polysilicon ion implantation (phosphorous) <p>Week 3</p> <ol style="list-style-type: none"> 1. Mask #3 + Lithography: define gate 2. Reactive ion etch (RIE) of polysilicon: SF₆ @ 100mTorr, 250W, 4 minutes 3. Gate oxide etch with BOE <p>Week 4</p> <ol style="list-style-type: none"> 1. Photoresist removal 2. Mask #4 + Lithography: define NMOS S/D and PMOS substrate contact 	<p>Week 4 (Cont.)</p> <ol style="list-style-type: none"> 3. Phosphorous implantation: NMOS S/D and PMOS N-well contact 4. Photoresist removal 5. Mask #5 + Lithography: define PMOS S/D and NMOS substrate contact 6. Boron implantation: PMOS S/D and NMOS substrate contact  <p>Device cross-section after PMOS and NMOS source and drain implantation</p> <p>Week 5</p> <ol style="list-style-type: none"> 1. Photoresist removal 2. Wafer Cleaning 3. Dopant activation annealing: N₂, 900°C. 4. Plasma enhanced CVD (PECVD) of silicon dioxide, 500nm 5. Four point probe sheet resistance measurement <p>Week 6</p> <ol style="list-style-type: none"> 1. Mask #6 + Lithography: define contacts 2. Oxide etch with BOE 3. Photoresist removal 4. Four point probe measurement <p>Week 7</p> <ol style="list-style-type: none"> 1. Wafer cleaning 2. Aluminum sputtering-deposition 3. Mask #7 + Lithography: define metal lines 4. Aluminum etch: H₃PO₄: HNO₃ (10:1) 5. Photoresist removal 6. Aluminum sintering: 390°C, 40 minutes  <p>Cross-section of the final CMOS structure</p>
Process Flow (cont.)	
<p>Week 8-10</p> <ol style="list-style-type: none"> 1. Device testing: PMOSFET, NMOSFET, Diode, Bipolar Transistor, Inverter, Ring Oscillator 2. Device characterization: <ul style="list-style-type: none"> - I-V and C-V measurement - Dielectric constant calculation - Mobility calculation 	 <p>NMOS and CMOS device results.</p>

'In its first offering by Chang, the course attracted the maximum number of students that the facility could safely accommodate. Renovations over the summer made it possible to increase the number to 20 students

per quarter (40 per year) . . . the lab lets students fabricate their own integrated circuits in the school's clean room facility . . . This experience is invaluable, and ensures them great career opportunities.'

INTERACTIVE WEBSITE

An interactive website is available to provide instructional modules on-line and outside the classroom [16]. The site contains sample homework and examination problems with solutions. It also provides information about the Semiconductor Industry and the current technology development. The purpose of this website is to provide students with up-to-date information on technological innovation and an 'up-to-minute' resume submission. All the senior undergraduate students who are taking CMOS processing course can choose to submit their resumes to this website and update their resumes regularly. The member companies have password-protected access to students' information for recruiting purpose. In other words, this website is a 'one-stop shopping' site for companies who want to:

1. learn about UC research in this field;
2. access students who are graduating with formal training in semiconductor manufacturing.

Additional links are provided to UC faculty and companies currently participating in this program.

SUMMARY

There is a need for curriculum innovation and integration in semiconductor manufacturing and engineering in training for chemical engineering students in the 21st century. This new multidisciplinary curriculum is an ambitious program that aims at the education and training, in Semiconductor Manufacturing, of engineering students from a variety of disciplines. This is a technologically advanced area of manufacturing that faces significant labor shortages. Up to forty students can be trained each year through this program. Students who have successfully completed this option are highly sought after by industrial recruiters and academic graduate programs nationwide.

Acknowledgement—I am indebted to Professor Robert Hicks at UCLA's Department of Chemical Engineering for his contribution about establishing this undergraduate option. I acknowledge the NSF Career Award (CTS-9985511), Intel, Lucent Technologies, Applied Materials, AMD, and Vitesse Semiconductors, UC-SMART, UC Instructional Improvement Office, and the staff at the Microelectronics Fabrication Laboratory and the Nanoelectronic Research Facility for supporting the development of this undergraduate teaching laboratory.

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