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Microelectronics Process Engineering at San Jose State University: A Manufacturing-oriented Interdisciplinary Degree Program*

EMILY ALLEN, STACY GLEIXNER, GREG YOUNG, DAVID PARENT, YASSER DESSOUKY
San Jose State University, San Jose, CA, 95192, USA. E-mail: elallen@sjsu.edu

LINDA VANASUPA
Department of Materials Engineering, California Polytechnic University, San Luis Obispo, CA, USA

San Jose State University's new interdisciplinary curriculum in Microelectronics Process Engineering is described. This baccalaureate program emphasizes hands-on thin-film fabrication experience, manufacturing methods such as statistical process control, and fundamentals of materials science and semiconductor device physics. Each course of the core laboratory sequence integrates fabrication knowledge with process engineering and manufacturing methods. The curriculum development process relies on clearly defined and detailed program and course learning objectives. We also briefly discuss our strategy of making process engineering experiences accessible for all engineering students through both Lab Module and Statistics Module series.

INTRODUCTION

HIGH-TECH MANUFACTURING companies use similar thin film processing methods to make components for electronics, information processing, communication devices and increasingly microfluidics and micromechanical devices. Process engineers are the personnel needed to *develop, maintain, monitor, evaluate* and *improve* processes used in these manufacturing environments. The interdisciplinary background needed by process engineers in various high-tech industries is practically identical, and establishes the need for process engineers to be educated specifically for 21st-century manufacturing industries.

In a 1991 Semiconductor Research Corporation (SRC) report [1], industry leaders suggested that microelectronics curricula should include more emphasis on process control and statistics, design of experiments, yield management and total quality management, as well as process integration and device physics. In addition, their concerns have been echoed by more traditional manufacturing companies, who have identified 'competency gaps' in engineering graduates [2, 3]. They see a need for students who are more practiced at working in teams, communicating effectively and using common sense to solve problems.

The Microelectronics Process Engineering Program (μProE) at San Jose State University has been designed to educate engineers in microelectronics fabrication as well as to address some of these missing elements in traditional curricula. μProE is a new interdisciplinary bachelor's degree program with an emphasis on microelectronics fabrication as a manufacturing process. Our goal is to produce graduates with the technical background to understand both the devices being produced and the processes by which they are manufactured. This bachelor's degree program includes coursework from the traditional disciplines of electrical, chemical, materials and industrial and systems engineering, as well as a laboratory course sequence in which integration of the disciplines is explicitly achieved. The curriculum has been initiated as a Concentration in the interdisciplinary General Engineering degree program. Because the program has begun with a relatively small enrollment (25 students in Fall 2001), the curriculum must utilize courses from other departments that are not necessarily a perfect fit. When the enrollment grows, more courses designed specifically for the program may be initiated. Below we describe the curriculum design process, the core laboratory course sequence and the lab and statistics modules.

μPROE CURRICULUM DESIGN

The μProE curriculum is designed to produce graduates with certain attributes. To impart these attributes, a set of forty-five program objectives (POs) were established. Table 1 lists just a few of these program objectives as examples. To meet

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Table 1. Examples of μProE program objectives. Program objectives fall into eleven 'outcomes' areas which are common to engineering programs

Outcome	Program objective: graduates of μProE program should be able to . . .
1. Ability to apply knowledge of mathematics, science and engineering	1.1 Make all required calculations for predicting and designing process steps (e.g. diffusion, ion implant, etc.).
	1.2 Make effective estimations and assumptions where necessary and document reasoning.
	1.3 Compare analytical calculations with simulated results and tabulated data.
2. Ability to design and conduct experiments and analyze and interpret data	2.1 Use statistical design of experiments and response surface methodology to characterize and optimize a process.
	2.2 Design a metrology procedure to characterize a process or device.
	2.3 Select appropriate measurement techniques to characterize a process.
	2.4 Capture limitations and error ranges of measurement tools.
4. Ability to function on multidisciplinary teams	4.1 Designate team roles and assign and monitor specific tasks of team members.
	4.2 Resolve conflict within team.
	4.3 Self-assess performance of assigned roles within team

Table 2. Examples of course learning objectives from MatE/ChE 166

MatE/ChE 166, Advanced Thin Film Processes

After successfully completing the course assignments, lab assignments, reviewing lecture notes, participating in class discussions, homework assignments, lab activities and examinations, a student should be able to . . .

1. *Detail* different ways of measuring surface roughness and identify the best measurement technique for different situations.
2. *Calculate* the evaporation rate of a pure metal.
3. *Calculate* the diffusional flux of material in a PVD process.
4. *Describe* the difference between accuracy and precision of a measurement technique.
5. *Calculate* the precision of a measurement technique.
6. *Quantify* the variation between users for a given piece of equipment.
7. *Design* an experiment using proper replication, randomization, and control of variables.
8. *Calculate* the variation between levels using a sum of squares method.
9. *Calculate* etching rate as a function of directionality and selectivity.
10. *Calculate* the mass balance of an etch process for endpoint detection.
11. *Identify* the rate limiting step during different stages of CVD.
12. *Describe* the oxidation/reduction reactions that occurs in electrolytic plating
13. *Identify* the variables that effect plating rate and film quality.
14. *Define* electromigration and explain its impact on IC reliability.
15. *Identify* mechanical integrity issues associated with metal and dielectric stacks.

Table 3. Examples of course learning objectives from MatE/EE 167

MatE/EE 167, Microelectronics Manufacturing Methods

After successfully completing the course assignments, lab assignments, reviewing lecture notes, participating in class discussions, homework assignments, lab activities and examinations, a student should be able to . . .

1. *Model* C-MOS process using TCAD (T-SUPREM4).
2. *Discuss* methods of reducing/controlling fixed oxide charge
3. *Extract* SPICE level 1 parameters.
4. *Extract* threshold voltage, gate oxide thickness, and body doping of PMOS and N-MOS transistors using CV plot data.
5. *Identify* sources of variation
6. *Describe* tools and actions which can minimize special cause and common cause variation
7. *Calculate* central line, upper and lower control limits for x-bar chart
8. *Determine* whether a process is or is not in statistical control

these program objectives, all courses and lab experiences must have student learning objectives (LOs). All LOs can be linked to POs and a master table recording these links is maintained for the purpose of assessing whether the program is meeting its goals. Future surveys of employers and alumni will allow us to make changes in POs when necessary and to adjust course learning objectives in turn. Courses typically have about one hundred learning objectives, which are written using Bloom's Taxonomy for educational objectives [4, 5]. Some example learning objectives are shown in Table 2 and Table 3.

Currently there are three courses (MatE/EE 129, MatE/ChE166, and MatE/EE 167, all described herein) which were designed specifically to meet program objectives for μProE. These three courses also enroll materials, chemical, electrical, mechanical and industrial engineering majors taking the courses as technical electives.

Table 4 shows the course requirements for the μProE degree. Many courses are cross-listed between departments and are team-taught by two or more faculty members from the various departments. Cross-listing also encourages students from

Table 4. Required coursework for interdisciplinary μProE degree

FALL	SPRING
1st Year	*1st year*
Calculus I	Calculus II
General Chemistry I	General Chemistry II
Introduction to Engineering (E10)	Physics I—Mechanics
General Education	
English Composition IA	English Composition IB
2nd Year	*2nd Year*
Calculus III	Differential Equations
Physics II—Electricity & Magnetism	Introduction to Circuits (EE98)
American Studies IA	American Studies IB
Introduction to Materials (MatE 25)	Statics (CE99)
	Oral Communication
3rd Year	*3rd Year*
Physical Chem. (Chem161A)	Matls Characterization (MatE141)
Systems/Structures Matls (MatE115)	Safety & Ethics in Engr. (ChE 161)
Electronic Props Matls (MatE 153)	Design of Experiments (ISE 135)
Engineering Statistics (ISE 130)	Semicond. Device Physics (EE128)
Technical Writing (E100)	**Basic IC Fab/Desgn (MatE/EE 129)**
Mass & Heat Transport (ChE 190)	Chemical Thermodynamics (ChE151)
4th Year	*4th Year*
Advanced Thin Film Processes (MatE/ChE 166)	**Microel. Manufacturing Methods (MatE/EE 167)**
Senior Design Project (E198A)	Senior Design Project (E198B)
Reactor Design/Kinetics (ChE158)	Solid St. Transformations (MatE152)
Technical Elective	Technical Elective
Advanced General Ed.	Advanced General Ed.

outside the μProE major to enroll in the core lab courses as electives.

μPROE LAB COURSE SEQUENCE

The μProE three-course lab sequence begins with Basic Integrated Circuits Fabrication and Design (MatE/EE 129), which has been extensively described elsewhere [6]. It is offered every semester and typically enrolls about 25 students. The course meets for two hours of lecture and three hours of lab per week; typically two lab sections are filled. Prerequisites include a course on electronic properties of materials. The lecture sections focus on basic integrated circuit processing and the fundamentals of metal-oxide-semiconductor (MOS) transistors. During the lab, student teams rotate between Fabrication and Test teams, (FATs) and Process Development teams (PROs). The FAT teams run wafer lots through a four-mask n-channel MOS process (N-MOS), handing off the product to the other team every two weeks with an oral status report. The PRO teams perform process design or process characterization experiments, concluding with a poster presentation every two weeks. During the semester, every student serves three times on a FAT team and twice on a PRO team. Students learn how to use all of the lab equipment, including aligners, spinners, furnace, wet benches, plasma etcher, evaporator, four-point probe and semiconductor parameter analyzer.

An innovative aspect of this course is the use of a fictitious corporate framework, Spartan Semiconductor Services, Inc (S3i). The course instructors act as the officers of the company, and the students are treated as employees. This fiction is maintained through the use of corporate 'memos' for all communications among students and between students and instructors. All equipment and process documentation is provided in an Employee Handbook. Problem-solving exercises are designed as customer specifications needing solutions, and the final exam requires each team to design a process flow and mask set for a 'customer' circuit. This pedagogical corporate framework provides an element of professionalism to the course, which is reflected in student work, pride of accomplishment, and an attitude of teamwork among faculty and students which differs markedly from the usual classroom. The S3i environment is used throughout the entire μProE course sequence.

After completion of MatE/EE 129, students are eligible to enroll in MatE/ChE 166, Advanced Thin Film Processes, and/or MatE/EE 167, Microelectronics Manufacturing Methods. These two courses bring in elements of design of experiments and statistical process control, respectively.

ADVANCED THIN FILM PROCESSES

The Advanced Thin Film Processes course (MatE/ChE 166) builds upon the previous foundation by introducing two focus areas: thin film deposition and characterization processes, and experimental design. The course, comprised of two 50-minute lecture periods per week and one three-hour lab section, has been offered during the Fall 2000 and Fall 2001 semesters, with about 8

Table 5. Laboratory modules for advanced thin film processes (MatE/ChE 166)

1. Using statistics and statistics software to analyze data
2. Quantifying equipment precision and developing standard operating procedures [7]
3. Quantifying the statistical variation in a process
4. Performing a single factor DOE and analysis of variance
5. Developing a 2^k factorial design
6. DOE using compounding and blocking

students enrolled each time. The lectures present advanced models for thin film deposition and etching and materials analysis. The course goal is for students to develop a deeper understanding of the physics and chemistry controlling thin film processes, as well as to learn to distinguish between various characterization methods. At the same time, students utilize their knowledge of these fabrication processes to develop Design of Experiments (DOE) and statistics skills needed for microelectronics manufacturing.

Table 2 shows some of the learning objectives for this course. The lecture component of the class covers materials analysis techniques, thin film reliability testing, evaporation, sputtering, chemical vapor deposition, electroplating, and plasma etching. The thin film processes investigated in both lecture and lab are not limited to those used in integrated circuit manufacturing, but may include films used in data storage, flat panel displays, or any other product area.

The laboratory sessions are divided into six lab modules, shown in Table 5, in which the students investigate important factors in designing robust experiments. Each lab module includes learning objectives, theory sections on the relevant thin film process as well as on statistics and DOE, 'dry lab' exercises, procedures for the thin film processing experiment, and assessment of the lab including student output (report or other assignment) and survey of student opinion on lab effectiveness. The lab modules are designed so that multiple small groups of students can learn the same manufacturing skill (such as designing and running a single factor experiment) on different thin film processes (such as evaporation, oxide deposition, or plasma etching). Because the student groups are working on different equipment, this framework provides the hands-on experience that comes from working in small groups, while still being able to accommodate a large class in one lab session.

In Lab Modules 1 through 3, students learn that statistics are a necessary tool to understand the variability that exists in microelectronics manufacturing. They use statistics to quantify the precision of a metrology tool and the variation that exists run-to-run in the processing tool. This builds student confidence in working with statistics and teaches them to analyze the validity of data. The labs also highlight a critical factor in designing experiments that students often overlook: the fact that the precision of the measuring tool and the control of the processing equipment need to be factored in when designing an experiment [7]. In Lab Module 4, students design and carry out a simple, single factor experiment. During the dry lab they perform a systematic design of their experiment including developing clear objectives, identifying all variables, and choosing levels that are appropriate based on the precision of the tools being used. Students use analysis of variance (ANOVA) to analyze data from different levels (such as high, medium, and low settings on the furnace) and determine if the levels are statistically different. The complexity of most thin film processes, and the need to examine more than one variable, is emphasized in this lab. Labs 5 and 6 build on the single factor experiment designed in Lab 4. Students utilize 2^k factorial DOE, compounding and blocking, to understand how multiple factors can be studied (and understood) simultaneously. The overall goal of the laboratory sessions is for students to develop a robust and practiced understanding of the important factors in designing an experiment.

As the laboratory facility grows and more processes become available, the Lab Modules may utilize new processes. DOE skills can be practiced on any process available, in our lab or in any other teaching laboratory. The Lab Modules have been written in a standard format to facilitate their adaptation by other users.

MICROELECTRONICS MANUFACTURING METHODS

The third course in the sequence, Microelectronics Manufacturing Methods (MatE/EE 167), combines complementary MOS (C-MOS) fabrication with statistical process control (SPC). Some example learning objectives for the course are shown in Table 3.

The course is comprised of two 50-minute lecture periods per week, one on statistical process control and the other on device physics and process modeling. MatE/EE 129 is a strict prerequisite for the course. The lab meets once a week for three hours. The laboratory runs with two teams that alternate duties between processing C-MOS circuits (FAT teams) and conducting SPC assignments in the lab (SPC task forces). This is a challenging manufacturing process to complete in one semester and can only be accomplished because students are already trained on the lab equipment. Several steps, such as ion implantation and chemical vapor deposition, must be purchased from outside vendors.

The C-MOS process used is based on an n-well process developed in the 1980's [8] due to its use of ion implantation and self aligned gate technology. We modified it to a p-well process so we could drop the channel stop implantation step. We wanted to introduce ion implantation, polysilicon growth and etch aspects, and photolithography of

Table 6. SPC tasks performed in MatE/EE 167

SPC task
1. Determine process variable (thickness)
2. Determine metrology tool
3. Identify the tolerance limits
4. Determine when to sample and sample size
5. Confirm that subgroups are rational
6. Compute sample means and sample ranges
7. Design trial range and x-bar charts
8. If special causes exist, analyze origins
9. Re-compute x-bar and range charts until special causes are eliminated
10. Determine process capability (i.e. C_p, C_{pk})
11. Determine process yield

modern C-MOS processing, without burdening the lab with too much off-line processing. The process was designed and simulated for 1.5-micron features with TSUPREM-4 (Silvaco's Athena).

While the FAT team processes the C-MOS lots, the SPC task force performs analysis on the simpler N-MOS process (used in the MatE/EE 129 course, which runs simultaneously but on alternate days). During the Spring 2001 semester, the task forces analyzed the field oxide, gate oxide, spin-on doping and metallization steps.

SPC lectures focus on the use of control charts to minimize within wafer variation, between-wafer variation, and between-lot variation for various processes. Table 6 lists the steps carried out by the task forces in conducting an SPC analysis. An example SPC project is an analysis of our wet field oxidation process. The students in MatE/EE 129 noticed a large variation in the field oxide thickness, and needed to know if they had to repeat the field oxidation step. They asked the SPC task force to conduct SPC analysis on the expected yields due to this variance, and to offer advice on how to improve the process. The results from the task force showed that the yields should still be above 90% even with the variance encountered, and that the large special cause variation was due to a temperature gradient in the furnace. This allowed the students in the N-MOS processing course to continue processing their wafers, thus preventing wasted lab time by starting over. The SPC team also came up with a solution to the temperature gradient problem.

The SPC task forces have to collect the data from the various N-MOS lab sections, and answer the following questions given upper and lower limits for the process:

- Is the process under control?
- If there is special cause variation, what is the cause?
- If nothing is done to improve the process, what will our yields be?

The students present their findings in oral and written reports.

The final project for this course includes extensive testing of the various inverter circuits and components.

μPROE MODULES

Lab modules

The μProE program has initiated other components in addition to the laboratory core sequence. We provide opportunities for all engineering students to learn about microelectronics processing through the use of μProE lab modules. Lab modules are hands-on experiences designed for a one-time, 3-hour lab session. Such lab sessions can fit into existing engineering and science lab courses to provide enrichment and recruitment opportunities, particularly in 1st- and 2nd-year courses. About 250 students per semester attend a lab module. These are primarily students enrolled in Introduction to Materials (MatE 25) and Electronic Properties of Materials (MatE 153). Currently they spend one lab session utilizing photolithography techniques to fabricate souvenir wafers. We are developing a solar cell fabrication module for freshmen engineering classes (E10). This academic year E10 classes spent one lab session testing solar cells and solving a design problem; next year these classes will have a session in the lab during which they perform the final lithography and etch step on their own solar cells before testing them. The purpose of the E10 solar cell module is to attract students to the μProE program and its course sequence. Other new lab modules are in development including one in which students fabricate a pressure sensor.

Statistics modules

A set of statistics modules is also under development for use in engineering statistics classes. Modern statistics textbooks may provide a variety of manufacturing examples to interest engineering students, from aircraft manufacture to electronic component testing [see, for example, Reference 9]. Our statistics modules provide case studies in DOE and SPC using microelectronics manufacturing processes. These modules can be easily adapted for any engineering statistics course as an accompaniment to a textbook.

Table 7 shows some of the modules developed for our Industrial and Systems Engineering courses. These case studies use data gathered either in our own lab or from the literature.

THE μPROE LABORATORY

The μProE Laboratory is designed around pedagogical objectives rather then research objectives. We install only equipment for which the maintenance and upkeep is feasible and which will be used for instructional laboratories. The lab is equipped with two proximity aligners, 3-stack tube furnace, DC sputterer, filament evaporator, wet benches, spinner, bake ovens, and a reactive ion etcher. All photolithography and etching is done in wet baths (except oxide etch). The lab is not a clean room but clean room

Table 7. Modules designed for engineering statistics classes

Course	Activity
Engineering Statistics (ISE 130)	T-test and confidence intervals for etch rate in RIE process Analysis of variance for thermal growth of SiO_2
Statistical Process Control (ISE 131)	Control charting for thermal growth of SiO_2
Design of Experiments (ISE 135)	2^K factorial design for CVD process

protocols are used (clean room jackets and gloves). Our laboratory and courses are designed to teach the fundamentals at a hands-on level; however, many of our students have co-op jobs and summer internships in state-of-the-art facilities in the Silicon Valley.

Improvements in the laboratory infrastructure and processing equipment continue to make courses easier to teach. A new de-ionized water system was installed recently, along with two new proximity aligners, one with backside exposure capability. Lab infrastructure improvements are scheduled for summer 2002. Equipment and infrastructure improvements have been made possible by our industry partnership program, which has provided significant funding for the laboratory.

USE BY OTHER INSTITUTIONS

The first course in the sequence (MatE/EE 129) has already been adopted or adapted by other universities. California Polytechnic University (San Luis Obispo) adopted the course in 1996. One author (LSV) develops statistics modules at her institution which we have used in one of our courses (MatE/ChE 166). The authors have received numerous requests for information about the original course and various faculty have adapted parts of it for their own use. The two new courses (166 and 167) should also be amenable to adaptation by other institutions. MatE 166, in particular, is designed so that any type of thin film process could be substituted in, while still utilizing the statistical applications and design of experiments approach. In addition, any type of manufacturing course could adapt our statistics modules.

FUTURE DEVELOPMENTS

The μProE courses are very expensive to teach, both in terms of laboratory costs and faculty effort. Because SJSU does not have Ph.D. programs, we suffer from a lack of long-term graduate students to staff the lab and teach lab sections, resulting in a heavy faculty workload in the lab. We have begun a system of structured lab training workshops for interested undergraduates and masters students. The two-day workshops provide opportunities for students to be certified as independent users of various tools and workstations in the lab. Eventually we hope this training program will provide us with a steady source of assistants for lab modules and courses.

The first graduate of the program finished in May 2001 and is now working at one of our partner companies. We now have 25 students majoring in the program; when these students reach their Senior Design course, the next challenge will be supervising such a large number of independent design projects in the laboratory. However, these projects can be used to make processing improvements and bring new equipment on-line.

CONCLUSIONS

The μProE program at SJSU has been operating for only two years, although the basic fabrication course has been operating for over seven years. We have successful N-MOS, P-MOS, and C-MOS processes and mask sets. A solar cell process has been designed and is currently being tested for large-scale robustness. We have designed three laboratory courses which teach teamwork, communications, statistical process control and design of experiments, alongside semiconductor device physics and manufacturing. The integration of statistics applications and manufacturing teams with the technical content of each course has been very successful to date. We look forward to continued expansion of our laboratory and new opportunities for interacting with local industry.

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Emily Allen is Chair of the Department of Chemical and Materials Engineering at San Jose State University. She teaches courses on electronic materials, IC processing and solid state kinetics, and conducts research on magnetic thin films and semiconductor processing. She received her Ph.D. in Materials Science and Engineering from Stanford University in 1992. She can be reached at elallen@sjsu.edu.

Stacy Gleixner is an Assistant Professor in the Department of Chemical and Materials Engineering at San Jose State University. She teaches courses on electronic materials, solid state kinetics and thin film deposition. Her research focuses on development and processing of microelectromechanical devices. She received her Ph.D. in Materials Science and Engineering from Stanford University in 1998. She can be reached at gleixner@email.sjsu.edu.

Greg Young is Assistant Professor in the Department of Chemical and Materials Engineering at SJSU. He received his Ph.D. in Chemical Engineering from the University of California at Davis in 1990. He teaches transport and semiconductor processing courses and conducts research on electroplating of copper. He can be reached at glyoung@email.sjsu.edu.

David Parent is an Assistant Professor in the Electrical Engineering Department at SJSU. He teaches C-MOS processing and device physics and conducts solar cell research. He received his PhD in Electrical Engineering in 1999 from the University of Connecticut. He can be reached at dparent@email.sjsu.edu.

Yasser Dessouky is an Associate Professor in the Department of Industrial and Systems Engineering at SJSU. He received his PhD in Industrial and Management Systems Engineering from Arizona State University in 1993. He teaches statistical process control and conducts research on operations management. He can be reached at ydessouk@email.sjsu.edu.

Linda Vanasupa is a Professor of Materials Engineering at California Polytechnic University at San Luis Obispo, and teaches electronic materials and processing. Her research is on characterization of metal film deposition. She received her Ph.D. from Stanford University in Materials Science and Engineering in 1990. She can be reached at lvanasup@tuba.calpoly.edu.