

Design and Successful Implementation of an NSF Research Experiences for Undergraduates site in Semiconductor Manufacturing*

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During 1999 and 2000, a National Science Foundation (NSF) sponsored site was established for Research Experiences for Undergraduates (REU) at the University of Central Florida (UCF). Each year, the REU program exposed 10 undergraduate students to educational and research experiences in such areas as robotics/automation, nonlinear modeling and advanced control, image processing, computer-aided integrated circuit designs, and computer networking. The REU participants undertook intensive study in their focus subject and under the supervision of their faculty advisors, conducted fundamental research, and interacted with our industrial partners toward implementing their ideas in the real world. A total of 20 projects were performed together with support from industrial and governmental agencies. This paper outlines the program, educational components, research outcomes, and experiences gained.

INTRODUCTION

THE FUTURE of our society will be shaped by the young and talented minds going through our colleges and universities today. As a part of our continuing effort in enhancing quality of undergraduate education and in getting undergraduates involved in research, several initiatives have been undertaken in Electrical and Computer Engineering at the University of Central Florida over the last several years. For example, multidisciplinary senior design courses with interaction with local industry, an NSF site of research experiences for undergraduates (REU), course-curriculum-and-laboratory improvement, etc.

Objectives of the REU program funded by NSF in years 1999 and 2000 are:

- To encourage more talented undergraduates, especially women, minorities and persons with disabilities, to pursue graduate studies in the above-mentioned areas in Electrical Engineering and Computer Engineering.
- To expose students to a stimulating research environment, where they will be encouraged to think creatively and to develop independent research skills that are useful regardless of their future career paths.
- To have students participate in real-world projects where they work as a team member with faculty members and our outside partners (from both industry and governmental agencies) and

learn to make engineering tradeoffs in designing and implementing electronic circuits and electrical systems.

- To train students in such fundamental ethical issues as obtaining, interpreting and reporting the results of their scientific work.
- To increase students' exposure to the state-of-the-art developments in the fields of their interest through site visits and interaction with industry, government agencies, and educational and research institutions.
- The specific technical focus areas of the program are microelectronic circuit design, robotics and automation, and semiconductor manufacturing. The areas are chosen based on our faculty research strengths *and* collaborations with local and outside experts. Participants and collaborating parties include:
 - Lucent Technologies, Orlando, Florida, semiconductor manufacture division;
 - Oak Ridge National Laboratory, Tennessee, microelectronic devices and circuits group;
 - Air Force Research Laboratory, Dayton, Ohio, microelectronics group;
 - Georgia Institute of Technology, computer integrated manufacturing systems;
 - Bethune-Cookman College, applied science and engineering;
 - Lockheed Martin, Orlando, Florida, robotics and simulation group;
 - University of Central Florida, mechatronics group, mechanical, materials and aerospace engineering;
 - Microtronic Inc., Orlando, Florida

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ACTIVITIES FOR REU STUDENTS AND ASSESSMENTS

To get REU students prepared to play an active role in one of the REU research projects, the following activities are scheduled.

- *Introductory courses.* An introductory course, specially designed for undergraduate students, was offered on modeling, control, robotics and automation. The second course was on semiconductor circuits and computer-aided design. These courses are to give REU students enough background in the aforementioned areas, and it will be offered in the first month of the summer.
- *General research seminars.* Parallel to the introductory courses, the graduate research assistant will conduct three research seminars to update the student's skill in conducting research and development. The first seminar is on literature searching, including research articles, patents, books, and reports. The second seminar is on the use of computer software such as ATLAS (from Silvaco International), PSpice (from Cadence Design Systems, Inc), Matlab (from The MathWorks, Inc.), MatrixX (from Wind River Systems), Labwindows (from National Instruments), etc. The last seminar is on common hardware and instruments.
- *Seminars on research topics.* To facilitate the selection of research topics by the REU students, a number of research seminars are offered on potential research topics, many of which are extracted from ongoing research projects.

Upon completing the three training items, REU students devoted a substantial portion of their time to their individual research projects. A summary of the REU projects is provided below.

To make the research experience of REU students worthwhile and challenging, the following three levels of advising and mentoring were used: Responsible Faculty Members, Research Assistant, and External Experts. To efficiently and effectively help REU students in carrying out their research, the following phases of interaction were carried out:

- *Background materials.* As elaborated above, faculty and graduate assistant conduct short courses and training to prepare REU students for research projects.
- *Selection of project.* Upon completing the course and training, the REU students visit several sites and listen to the presentations by the faculty and their collaborators on the student projects. Then, REU students meet with their respective advisor to select a project and to set up a schedule for completing their participation in the REU program. Our goal for these first two phases is to spark student's interest in proposed research projects. Once started, the REU students are encouraged and challenged through regular interactions in the remaining phases.

- *Regular office hours.* Each participating faculty member provide 3 to 5 office hours per week strictly for REU students during which time the students can ask questions and discuss their projects. The graduate research assistants also have office hours between 10 to 15 hours every week for REU students who have questions regarding computer simulation, basic design techniques, etc.
- *Remote interaction.* Accounts are established on the workstations in the Robotics Laboratory and Microelectronic CAD Laboratory so that REU participants can communicate using the Internet with off-campus engineers/experts (including faculty members from their home institutions) and report to them their progress. The REU website also enables students to share information about their progress and for us to disseminate the results.
- *Weekly project meeting.* The faculty members hold weekly meetings during which each of the REU participants will discuss their research progress.
- *Biweekly REU group meetings.* Once the REU students have made significant progress on their research projects, a group meeting is held every other week during which each student gives a status report. Since the research projects address different aspects in process automation, integrated circuit (IC) designs, and computer networks, the group meeting bring together all of the REU research projects being carried out independently by the REU participants. These meetings are run by students for themselves to encourage questions and exchange of ideas. The purpose was to foster team spirit among the REU students.
- *Project defense.* At the end of their program, all projects are defended by the REU students. A panel consisting of faculty advisors, internal and external experts will evaluate their performance regarding all aspects of research such as literature search, understanding of the topic, problem-solving approach, simulation or experimentation, technical writing, and ability of oral presentation. The project reports together with the panel evaluation are made available on the web.

EDUCATIONAL COMPONENTS ON SEMICONDUCTOR MANUFACTURING

The site focused upon semiconductor manufacturing. The main objective is to provide a multi-disciplinary environment and for the students to gain hands-on experience of several key aspects of semiconductor manufacturing process. Short courses, seminars, and case studies (extracted from ongoing research projects) cover many subjects of semiconductor manufacturing education and research, including (but not limited to) the following:

- Modeling of machine tools for semiconductor manufacturing, material handling in manufacturing, design and networking of machine tools.
- Semiconductor device modeling, circuit designs, processing and fabrication, packaging, and reliability analysis.
- In-situ monitoring, inspection, and quality control (by means of dynamic modeling or optical character recognition and image processing).
- Intelligent control systems for automating manufacturing process.
- Advanced circuits design and analysis for biomedical application and wireless communication.

Introductory courses

In the first introduction class, kinematic and dynamic modeling of machine tools, their control and automation are covered. Specifically, the following subjects are covered within two weeks:

- *Kinematic modeling.* Given the joint variables and geometry of the machine, find both position and orientation of the machine tool in the workspace. The kinematic solution can be used to develop inverse kinematic mapping, Jacobian (velocity mapping), and acceleration mapping. The discussions of kinematic modeling are done using both homogenous transformation of typical joints [1] and Denavit-Hartenberg convention [2].
- *Dynamic modeling.* Upon having the kinematic relationship, kinetic and potential energy of the machine can be analytically expressed, and a dynamic model can be derived using the Lagrange formulation [3].
- *Control and automation.* Trajectory planning algorithms are discussed, and common feedback controls such as PID (proportional integral derivative) and computed torque controls are studied. Other useful control methods such as position and force control, impedance control, cooperative control, robust and adaptive controls are also outlined.

A robotic wafer handling system consisting of a cassette sorter, a loading/tilt station, and a robotic manipulator is used as an example. Matlab files for simulating any 6-DOF (degree-of-freedom) rigid body motion and control are given to REU students. This short course provides REU students sufficient background in understanding how an automated manufacturing process can be analyzed.

The second short course focuses upon semiconductor device modeling, device and circuit simulation, analog/digital circuit analysis and design. Specifically, it deals with device physics, model development and circuit simulation, and it covers semiconductor device models implemented in PSpice. Emphasis is placed on CMOS (complementary metal-oxide semiconductor) device modeling, CMOS digital and analog circuits, and mixed circuits for wireless applications.

CASE STUDIES

After taking the short courses and the general seminars on literature search and usage of hardware and software in the laboratories, the REU students then selectively go through some of the case studies. These case studies, taught jointly by faculty advisors and their graduate students, are intended for two purposes: further illustration of research components and process, and introduction of specific research topics for REU students. These case studies cover the general areas listed above. In what follows, a few samples of these case studies are outlined.

Intelligent, fault-tolerant and robust control for autonomous robots in semiconductor manufacturing

Semiconductor manufacturing is moving into sub-micron technology that requires class-10 classrooms. In the near future, restrictions on particle counts will force operators out of manufacturing areas. Autonomous robots will then be needed to handle materials and supplies. As such, new real-time control algorithms and control hierarchy need to be developed for robots in a virtual manufacturing cleanroom, and it will have such capabilities as reasoning, collision-avoidance, trajectory planning, fault tolerance against sensor failures, robust and adaptive control against an uncertain/changing environment. One of intelligent control structures, discussed in details and originated from [4] and references therein, consists of the following layers/components:

- Local control at the process/component level (local level).
- Individual estimation, monitoring, and inspection devices (local level).
- Discrete monitoring and fault-recovery control (regional network level).
- Intelligent reasoning and control (overall system level).

Research components along this line include development and integration of robust control, adaptive control, fault-tolerant control (including novel ways of sensor integration), force controls, and intelligent controls for mobile robots maneuvering between processing stations in the cleanroom.

Process monitoring, modeling, prediction and control to increase yield

IC manufacturing involves hundreds of sequential steps on silicon wafers, each one of which could lead to yield loss. To maintain product quality and reduce yield loss in IC manufacturing, it is necessary to monitor and control various process variables. In particular, one can study particles and their effects in silicon wafer plasma etching processes by focusing upon the following areas in order to achieve the goals of high yield and high quality:



Fig. 1. Reflectivity of different wafer layers.

- process monitoring and process modeling;
- process optimization and real-time process control;
- diagnosis and prediction for reducing equipment cleaning frequency.

The emphasis is placed on the central subject of particle formation, modeling and monitoring as it is one of the most important issues affecting production quality and yield. To this end, the options of particle monitoring are discussed: in-situ particle monitor to detect particles in process chamber using either bright-field or dark-field sensing, or surface scan for particle counts on test wafers. For example, to understand particle formation in the chamber and to predict and optimize the purge and pump-down procedures, modeling of particles and their effects in an IC process can be done using particle information from both dark-field particle sensor and surface scanner. While particle counts on test wafers provide information about the impacts on quality and yield and can also be used as periodic calibration, an in situ sensor provides information about dynamics of particle formation in the chamber and hence generates a good signal indicating high-particle events such as particle avalanche. In a plasma chamber, particles form from the etching process and begin to float in the gas, and they either pass through the chamber or get dispersed onto the wall (and wafers), and as the particles accumulate on the wall, avalanches will eventually occur. It would be ideal that equipment cleaning be done before the onset of a major avalanche but not too soon.

Thus, predicting onset of an avalanche offers benefits in increasing yield without much detrimental effects on wafer quality in the IC process. Although dynamics of avalanche are not well understood, there are two ways we can use to gain understanding about avalanche. One is to model avalanche as a local scenario in which displacement of some unstable parts of material leads to a collapse through amplitude amplification. The other way is to think avalanche as a

de-localized motion mechanism in which thin slices of material get destabilized and start to slide.

Existing results on avalanche models for granular materials [5] are discussed, and possible research topics are illustrated. For instance, particle buildup may not be continuous as wafers are processed in batches; the avalanche model being sought is primarily for predicting the onset of avalanche(s) rather than the dynamics of the avalanche after its onset; there could be more than one avalanche in the chamber, and particle sizes are important; and gas pressure and flow in the chamber should have a significant impact on particle motion and avalanche, and the main cause of particle buildup needs to be identified.

Inspection and quality control using optical character recognition and image processing

In semiconductor manufacturing, all wafers are tracked and inspected throughout the fabrication process. Specifically, wafers are identified using their serial numbers (on the front and back sides) and sorted before each processing recipe is applied, and they are inspected again for quality control. For this purpose, image acquisition system and robust algorithms must be designed to achieve readability of wafers, especially, those containing optically damaged characters and/or with thick chemical layers.

The semiconductor industry has desired for many years to optically and fully automatically read the serial numbers of its semiconductor wafers and has made the transition from barcode marks to optically inscribed serial numbers (numeric and alphabetical characters) or dot matrices. While the optical character reading (OCR) has successfully been implemented using commercially available software and hardware, further integration and improvements are needed. In this case study, advantages and drawbacks of the existing technology are investigated, and directions of further development are identified so that productivity can be improved in wafer handling



Fig. 2. Wafers with damaged characters.

and processing. Specifically, optical characteristics of various wafers (including control wafers and wafers that are optically damaged) are studied to determine efficiency of the light mechanism, optimal illumination is sought toward the goal of making all wafers readable by OCR with minimum (none if possible) tuning of its intensity, and new image processing algorithms need to be implemented to improve readability of OCR. For example, Fig. 1 shows the images of wafers with low and high reflective layers, respectively; and Fig. 2 contains images of damaged characters.

Once OCR is done successfully, inspection can be proceeded with by analyzing the same wafer image. The goal of quality control is to identify defects on the wafer being processed. Figure 3 shows the result of whole-wafer surface inspection and, depending on the outcome, micro inspections may be needed. Inspection is often done by comparing the acquired image with the 'expected' one (called the golden wafer) or the one obtained

last time. Such a comparison can be implemented using the thresholding technique [6]. Specifically, algorithms that automatically compute an appropriate threshold level (for instance, mean value, or two peaks, or edge pixel, or iterative selection, or fuzzy entropy measuring, or fuzzy Yager measuring, or min-square error) can readily be adapted for damage/defect inspection. That is, the areas (highlighted in Fig. 3) whose contrast to those of the golden wafer exceeds the threshold values are labeled as defects.

As the next step in quality control, defects and their occurrence can then be modeled in order to identify their cause. Such a modeling can often be done by first classifying the defects according to size, shape, recipe, and other attributes in a database and analyzing the database entries using statistic correlation. Defects detected may not confirm with prescribed shapes. To classify them, edge information (that is, geometric shape, size, location and orientation) must be determined.

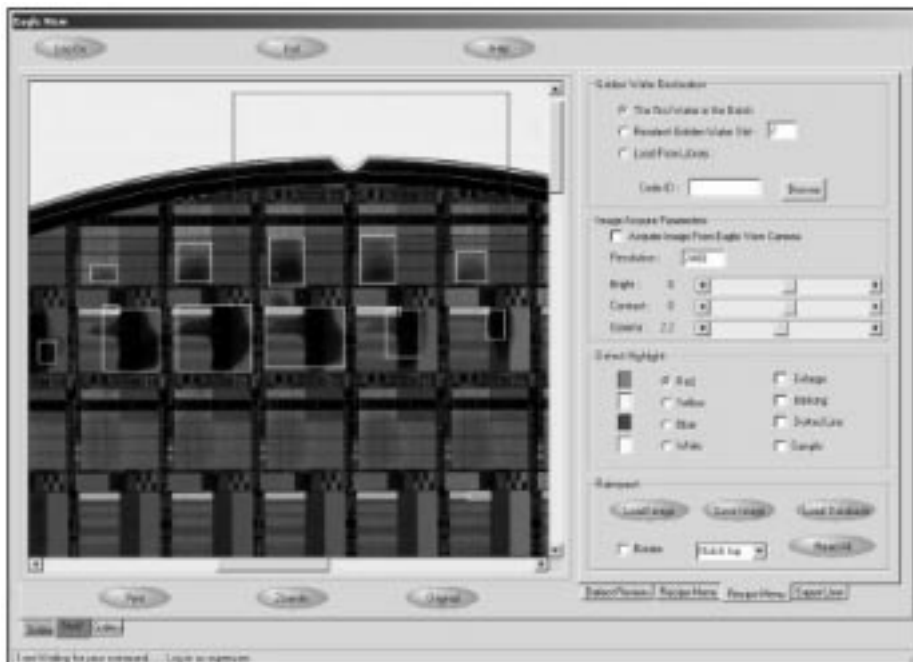


Fig. 3. Surface inspection of wafers.

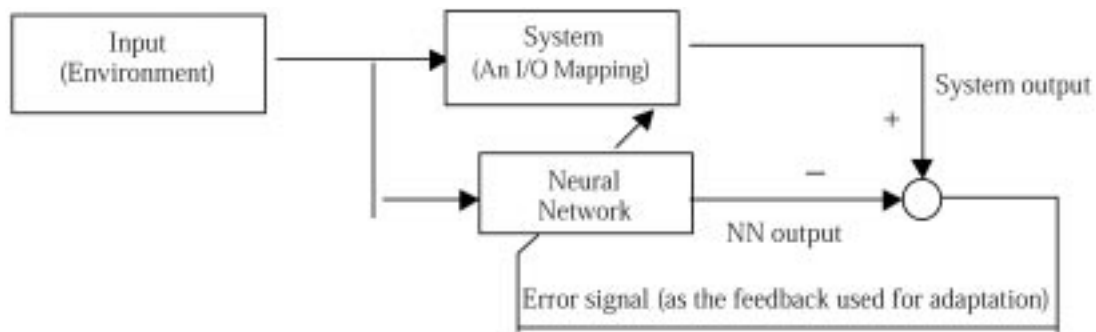


Fig. 4. Block diagram of neural network supervised learning.

Common edge-detection algorithms (for example, gradient differential method, morphological operation, and Sobel and Canny edge detection techniques) are introduced, and different types of classifiers (linear, nonlinear parametric, or non-parametric) are mentioned.

A neural network framework for high-level modeling and decision making

A neural network is a massive interconnection of computing cells (artificial neurons) designed to imitate the way the human brain learns and performs various tasks [8]. To attain a desired learning objective, synaptic weights (also called parameters) of the network of artificial neurons are modified through training. The so-called back-propagation algorithm [7] is arguably the most popular way to train a multi-layer neural network, and its mathematic formulation is reviewed to illustrate the basic idea. In short, the back-propagation algorithm consists of applying the steepest descent method to the mean square error between the desired and the actual outputs (in order to minimize the error through adjusting network parameters).

A common paradigm of neural network learning is *supervised learning* or *learning by error*, and its closed loop block diagram is depicted in Fig. 4. The network is trained by applying a large set of input/output samples. The network parameters are updated to minimize the difference between the desired response and the actual response of the network produced by the input, in accordance with an appropriate criterion. For system modeling and control, neural networks are natural candidates to approximate and represent an unknown relationship between a set of inputs and a set of outputs.

Progress on applications of neural networks is surveyed, with emphasis on automation and optical character recognition [9].

REU STUDENTS, REU PROJECTS AND RESEARCH OUTCOMES

In this section, information about REU students is summarized, and abstracts of REU projects are provided. These projects deal with robotics and automation, manufacturing, microelectronic circuit designs, and their applications. Impacts of these results are discussed as well. Information about REU students is given in Table 1.

Summary of REU projects

- *Project 99-1: Trajectory Planning, and Control Algorithms for Autonomous Optical Character Recognition Robot in Semiconductor Manufacturing.* Outline: Semiconductor manufacturing requires inspection of wafers. In this project, dynamics of an OCR inspection robot is derived, and computed-torque control is designed. A real-time trajectory planning algorithm is developed and tested.
- *Project 99-2: Simulation and Visualization of Autonomous In-Cassette Reader.* Outline: A new configuration is designed for autonomous in-cassette reader of silicon wafers. Matlab is used to simulate dynamics and control of the system, and Labwindow GUI (graphical user interface) is developed for visualization and for potential real-world implementation.
- *Project 99-3: Material Handling of Flexible Materials and Testing.* Outline: For study and testing of flexible materials used in manufacturing, kinematics of a Stewart platform installed at UCF is investigated so that the platform can be used a test bed for measuring vibration induced by material handling. A Labwindow GUI is developed to interface with MEMS (micro-electrical-mechanical-system) sensors, to collect the data, and to perform various data processing functions.

Table 1.

Total #	Gender	Race and ethnicity	Citizen and P. resident	Class
20	Male 17 Female 3	Asian 3 Black 3 Hispanic 3 Non-Hispanic White 11	20	Junior 3 Senior 17

- *Project 99-4: Design and Simulation of an End Effector for Dexterous Manipulation.* Outline: A specific design of an end effector is developed for the Advanced Life Support Automated Remote Manipulator (ALSARM) built by UCF for NASA. Kinematics, Jacobian and dynamic equations are derived for the end effector. Matlab is used to simulate of its motion.
- *Project 99-5: Development of Bioluminescent Bioreporter Integrated Circuits (BBICs).* Outline: Working with scientists at the Oak Ridge National Laboratory (Tennessee), a BBIC is designed and prototyped, in which whole-cell bioreporters engineered for bio-luminescence of a particular substance are placed on IC to detect light and process the signal. The advantages of such a sensor are low cost, low power, and compactness.
- *Project 99-6: Study of Genetic Mutations Using Micro-CAT (computerized axial tomography) Scanner.* Outline: Working with scientists at the Instrumentation and Controls Division at the Oak Ridge National Laboratory (Tennessee), the genetic mutations in mice are studied and determined. The large number of mice that needed to be studied at one time makes this project very time consuming and causes logistical difficulty. Hardware and software were developed to improve the efficiency of the study.
- *Project 99-7: Mixed-Signal Design Using Dimensional Analysis and VHDL-AMS (Very-High-Speed-Integrated-Circuit Hardware Description Language with Analog and Mixed Signals).* Outline: Working with scientists at the Information Technology Division at the Air Force Research Laboratory (Dayton, Ohio), symbolic matrix techniques and approaches are studied for mixed-signal design using dimensional analysis and VHDL language. The approach is implemented into circuit simulator PSpice, and simulations of RLC (resistive-inductive-capacitive) circuits are carried out to demonstrate the new approach.
- *Project 99-8: CMOS Circuit/Chip Design Using Cadence CAD (computer-aided design) Tools.* Outline: The design of 16×16 multiplier is studied by researching different architectures concentrating on addition and multiplication. This research was used in deciding which architecture is good at throughput in ASIC design. Synopsys VHDL is used for logic simulation.
- *Project 99-9: Implementation of the Substrate Noise Model in PSpice.* Outline: Numerical algorithms are studied to predict the CMOS ac lifetime using the Dominant Degradation Asymptote (DDA) method. The new DDA method can predict the ac lifetime more accurately than the conventional method. For a given technology, the degradation rate and the voltage-acceleration factor are extracted as a function of the oxide electric field.
- *Project 99-10: Gate Oxide Integrity in Small-Geometry MOS Transistors.* Outline: Hot carrier degradation in thin gate VLSI (very large-scale integration) circuits is investigated. Cadence PSpice simulation is used to study the CMOS inverter, NAND gate, and NOR gate. The NOR gate shows more hot electron degradation than inverter and NAND gate. The analog circuits such as current mirrors and different amplifiers subject to hot electron stress are also studied. Hot electron effect reduces the current mirror stability in predicting constant current over drain-source voltage.
- *Project 2000-1: Readability Study and Neural Network Algorithms for Optical Character Recognition.* Outline: In this project, readability of optically damaged characters is studied using statistical and deterministic measures to identify key features of semi fonts for robust OCR. Neural network algorithms such as Hebbian network have been used to enhance the robust template match algorithm being developed at UCF.
- *Project 00-2: Chaotic Circuits and Their Applications in Wireless Communication.* Outline: In this project, chaotic circuits such as Chua's circuit and Duffing chaotic attractor are simulated to understanding many of nonlinear phenomena. Synchronization, control design and observer design are studied for applications in secure wireless communication.
- *Project 00-3: Robust Control of a Nonlinear String System Arising from Handling of Flexible Materials.* Outline: In this project, a flexible system that includes a nonlinear stretched string supported on a transporter is considered. Robust control is designed using Lyapunov argument to damp out transverse oscillation of the string by compensating for possible uncertainties in string dynamics and transporter motion, and simulation is carried out using the finite difference method.
- *Project 00-4: Simulation, 3-dimensional (3-D) Visualization and Real-Time Web Support of a Manufacturing Robotic System.* Outline: In this project, a graphical user interface (GUI) is developed, and dynamic simulation and 3-D visualization of a robotic system are carried out. The GUI enables the user to access Matlab simulation, visualization, other supporting functions via web.
- *Project 00-5: Electromagnetic Interference on Integrated Circuits.* Outline: EMI measurement techniques and methodology are studied to measure EMI (electro magnetic interference) and EMC (electro magnetic compatibility) compliance at the package and IC levels.
- *Project 00-6: Digital Chip Simulation and Design.* Outline: Synopsys VHDL simulation is conducted to study digital chip design. The timing analysis of full adders, half adders, and shift registers are simulated and studied.
- *Project 00-7: Shallow Junction of Deep Sub-micron CMOS Devices.* Outline: Device physics of shallow junction and short channel effects of

deep submicron CMOS technologies are studied. The device design for feature size less than 0.18 μm is examined.

- *Project 00-8: Application of the Haar Wavelet Transform for Observing Tumors in Mammograms.* Outline: Working with scientists at the Air Force Research Laboratory (Dayton, Ohio), a new method based on the Haar wavelet theory is designed and developed to process the image for observing and tracking breast cancer. Such a method can improve the image resolution and reduce the time of image processing.
- *Project 00-9: Development of Improved Method for Testing the Electrostatic Discharge (ESD) in Semiconductor Devices.* Outline: Working with engineers at Intersil Corp. (Melbourne, Florida), the physical mechanism of ESD is studied and analyzed for MOS semiconductor devices. Based on the results, an improved experimental setup is then developed for the testing and measurements of ESD events in microchips. The new setup can provide an improved accuracy and efficiency in characterizing the ESD effects in semiconductor devices and integrated circuits.
- *Project 00-10: Mixed-Mode Simulation of Electrostatic Discharge Preventive Circuits.* Outline: Working with Intersil's engineers, a device simulator called Atlas is used to conduct the mixed-mode simulation (i.e., simulation at both the device and circuit levels) of various semiconductor devices and integrated circuits. In particular, mixed-mode simulation is carried out using Atlas to study the characteristics and performance of some widely used ESD preventive circuits subject to the ESD stress. The project has useful applications to the understanding of protecting microchips against ESD event and to the development of more effective ESD preventive circuits.

RESEARCH OUTCOMES AND THEIR IMPACTS

All the REU projects are completed with project final reports that summarize the background information, research objectives, methodologies, and simulation or implementation outcomes. And, each project is defended by the REU student in front of a panel that consists of faculty advisors, internal and external experts. REU student performance is evaluated regarding all aspects of research such as literature search, understanding of the topic, problem-solving approach, research results, simulation or experimentation, technical writing, and ability of oral presentation.

A majority of the REU students chose the topics that are related or derived from ongoing funded research projects. As such, their research indirectly contributed to the success of these projects. More importantly, REU students benefited directly from these funded projects in the following ways:

- REU participants can learn more and better through their involvement in one of the ongoing projects.
- REU participants can relate their own projects to the real world through these research ties.
- Ongoing projects provide the environment (for example, site visits, seminars, etc.) and support (in terms of guidance from outside experts, graduate students, etc.) that enrich the research experience of REU participants.

Besides research reports, several REU students continued their work with faculty advisors and graduate students and published archived journal articles [10, 11] and refereed conference papers [12–15].

CONCLUSIONS

The REU program at UCF has been carried out successfully and proven to be a challenging and rewarding experience for REU participants, their graduate mentors, and faculty advisors. Observations made and lessons learned are:

1. Pedagogically, it is necessary but challenging for faculty advisors to keep the REU students motivated, involved, interested while they go through the short courses due to their short time duration, in-depth and broad converges.
2. Once REU students move into the phase of research seminars and project selection, regular guidance from the faculty are needed to keep students focused and help them overcome hurdles.
3. REU students are more likely to choose a research topic that is a part of ongoing research project, enables them to talk to graduate students and engineers/scientists from sponsors, and convinces them of its practical importance.
4. While most REU project work can be done during the Summer semester, many of them could not complete their project report within the duration of 12 weeks from the start. As a result, project reports are collected in the following Fall semester with project defenses done in November. This extended timeline worked well.
5. Through properly screening of applications and on-site advising, all the REU students admitted are proven to be well motivated and very capable. They have diverse background: 2 are black, 3 are Hispanic, and 3 are women out of the total 20 REU students.
6. REU projects are of very good quality. Nonetheless, more work after completion of REU projects is needed in order to yield refereed publications. The extended work can be carried out by teaming up a REU student and a graduate student so their joint work becomes comprehensive.

7. The REU site provides an excellent avenue for motivating and recruiting domestic students to get into graduate programs.

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