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A Systematic Multi-Level Assessment Approach to Enhance Students' Academic Performance in Sequential Logic Design*

AWOS KANAN, RAJAA ALQUDAH and AMJED AL-MOUSA
Department of Computer Engineering, Princess Sumaya University for Technology, Amman 11941, Jordan.
E-mail: a.kanan@psut.edu.jo, r.alqudah@psut.edu.jo, a.almousa@psut.edu.jo

This paper presents a systematic student-level approach to assess the impact of problem-based learning on enhancing students' performance in an undergraduate Digital Logic Design course. The problem was assigned as a mini-project and chosen to strengthen the student's understanding of an advanced part of the course, namely the sequential logic design. The study included data from semesters where students were assigned projects and other semesters without projects. The proposed approach relies on dividing students into groups based on their academic performance level to study how the project impacts these groups' performance. A baseline performance metric was created at the beginning of the semester to classify the students into three groups. At the end of the semester, the students' groups were reassessed to capture performance changes. The results consistently showed improvement across all students' levels in the semesters where the project was conducted. While it is natural for students' performance to change between the beginning and the end of the semester, the results show that the percentage of students who improved their performance level has increased in semesters with a project compared to the semesters with no projects. Also, the percentage of students whose performance degraded by the end of the semester has decreased in the semesters with a project. These results were also supported by an independent student survey that confirmed the positive project impact on the students' grasp of sequential circuit design.

Keywords: problem-based learning; digital logic design; sequential circuits; engineering education; schematic simulation software

1. Introduction

Problem-Based Learning (PBL) [1] is an effective pedagogical approach that is widely applied in engineering education. PBL can be defined as a student-centered learning model where instructors act as facilitators in a self-directed learning environment that allows students to acquire new knowledge and apply it to tackle real-world problems [2]. Although the idea of using such real-world problems in the classroom is not recent, it has not received a common interest until the late 1960s when it has been first incorporated into medical education [3]. The approach then found its way into other fields such as law, architecture, and engineering. Meanwhile, Project-Based Learning (PjBL) is another well-known approach that is closely related to PBL in the sense that it relies on solving some real-world problems. A problem in PjBL is considered an initial step to gather and integrate new knowledge. The PjBL model is typically applied to complex and open-ended problems that require students to conduct investigations and make assumptions to solve them. While design projects are typical in engineering education, the categorization of a given pedagogical approach as PBL or PjBL is a challenging task, especially since there is no agreement in the literature on the boundaries between them. Moreover, the term PBL is sometimes interchangeably used to refer to Project-Based Learning making the two terms confused with each other [4].

The Digital Logic Design course is the first hardware-oriented course for a variety of academic programs in electrical engineering and computer science domains. It serves as a basis for more advanced hardware classes such as Computer Architecture, Microprocessors, and Embedded Systems. Traditionally, the content of this introductory course is delivered in the form of lectures to convey the subject knowledge using in-class discussions and examples. Applying advanced pedagogical approaches, including Problem-Based Learning, is more common in higher-level courses. Thus, introducing a course project for the first time constitutes a challenge for the students as well as the instructors.

Other challenges the educators of Digital Logic Design face are the students' low engagement, enthusiasm, and performance toward the end of the semester. This typically coincides with discussing advanced topics such as sequential circuits. The transition from the straightforward timing of combinational circuits in the first part of the course to the more complex state-based timing of sequential circuits is not smooth for the majority of students. Despite the fact that students' performance improves with doing more examples on the white-

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board supported by animation- based presentations, both direct (exam-based) and indirect (survey-based) assessments of the course show that there is a need for performance enhancement.

While it is established that PBL is effective in delivering engineering concepts, it is very critical to analyze its impact on students' performance, especially for this introductory course with high enrollment, different students' majors, and varying performance levels. Classical approaches for assessing the impact of PBL rely on lumping all students in one group, without segmenting them into performance-based groups. Studying the impact of PBL on different groups, as well as investigating its impact on the individual student's performance would help draw more precise conclusions and recommendations for continuous improvement at both the course and program levels.

In response to the aforementioned challenges, and motivated by the positive feedback on project-based courses offered by the Computer Engineering Department at Princess Sumaya University for Technology (PSUT) [5, 6], this article proposes a systematic multi-level assessment approach for a closer look at the impact of project-oriented PBL on students' performance in sequential logic design. The main contributions of the proposed work are:

(1) An investigation of the pedagogical challenges in developing, implementing, and assessing the proposed project.
(2) A baseline-based approach to determine students' performance levels.
(3) A systematic multi-level approach to assess the impact of the project on students from different performance levels, as well as individual students' performance changes.
(4) An indirect assessment of the proposed approach based on students' feedback in periodic surveys independent of this study.

The rest of this paper is organized as follows. Section 2 discusses the related work. A brief overview of the Digital Logic Design course at PSUT is presented in Section 3. Section 4 introduces the methodologies used to develop and assess the proposed approach. Assessment results are presented and discussed in Sections 5 and 6, respectively. Finally, Section 7 presents the conclusion and future work.

2. Related Work

This section presents related studies. Subsection 2.1 reviews the use of PBL and PjBL in enhancing the teaching of general engineering courses. Meanwhile, subsection 2.2 presents a review of pedagogical approaches proposed in the literature to enhance teaching the Digital Logic Design course.

2.1 Problem-Based and Project-Based Learning in Teaching Engineering Courses

The effectiveness of PBL and its impact on students' performance and problem-solving skills have been investigated in several studies [7–12]. The authors of [7] proposed an interdisciplinary methodology to enhance the outcome of engineering students. The approach was to organize students to work on teams and apply their knowledge to a real-world problem. The study shows that this approach positively affected students' performance, readiness for the job market, the number of patents registered by students, and the number of newly founded start-ups. The authors of [11] used PBL to bridge the gap some undergraduate engineering students had in applying the knowledge to real-world situations. Here, a practical problem was given to students to solve, collaborate and simulate a real-world experience. As a result, positive feedback was received from students about their experience through the process. Meanwhile, a two-way Analysis of Variance (ANOVA) data analysis method was used in [12] to study the effect of PBL on students' critical thinking skills. The results showed that students who used PBL have developed better critical thinking capabilities than students who were not exposed to PBL.

According to the discussion presented in Section 1, PjBL is another pedagogical approach that is closely related to PBL. The impact of PjBL on teaching electrical and computer engineering courses has been extensively investigated in the literature. In [13], the authors assessed the effectiveness of PjBL in teaching Computer Architecture. The study results concluded that with a project, students could achieve a more technical understanding of the material and develop skills like teamwork, initiative, and collaboration. The authors in [14] investigated how a PjBL approach can facilitate and promote self-directed learning among students in an undergraduate-level Embedded Systems course. Another PjBL approach to enhance teaching Embedded Systems using Field Programmable Gate Arrays (FPGAs) has been investigated in [15]. To bridge the gap between teaching Integrated Circuit Design courses and the industry needs, the authors in [16] proposed an approach to offer an industry-relevant project during the course. The specifications of this project were collected based on the course's basic requirements, industry demand, and the usage of industry design tools and methodologies. Results in the final exam showed that doing the project positively impacted students' grades in the integrated circuit

design questions. Several more PjBL approaches have been proposed and assessed in the literature, including [17–20] for Power Supplies and Photovoltaic Electricity, Power Electronics, Analog Electronic Technology, and Electrical Power Systems courses respectively.

2.2 Pedagogical Approaches in Teaching Logic Design

Many researchers studied the use of different pedagogical methods and technology tools to enhance the process and the outcome of teaching logic design concepts. The authors of [21] studied the impact of introducing the concept of programmable logic devices (PLDs) on the understanding level among Logic Design students. The study shows positive feedback from students on their experience learning about PLDs, which helps them understand the topics of digital logic design and computer architecture. Similar approaches to enhance teaching digital Logic Design using PLDS have been proposed in [22, 23]. In [24], the authors studied the impact of using the System for Digital Logic Design and Simulation (SDLDS) on teaching Logic Design Courses for undergraduate students. The SDLDS system helps students in designing and simulating switching circuits. After evaluating the use of this system among digital Logic design students, the study shows that the average grade in the final exam increased from 7.68 to 8.6 out of 10. In contrast, the percentage of passing students in the exam improved from 77% to 92%. A similar study in [25] shows the effectiveness of using virtual emulation tools in teaching advanced digital design concepts. In order to evaluate the benefits of giving digital design students unlimited access to programmable boards outside the classroom, the authors of [26] conducted a study at three different universities in three different countries. The study shows that unlimited access to programmable boards improves students' understanding of logic design concepts and provides an opportunity to improve their knowledge of modern design tools.

A web-based system for teaching and learning Digital Logic Design has been introduced in [27]. The proposed system has been realized on a client-server Java-based architecture with five modules to control all procedures needed to assess students and keep track of their progress. The authors of [28] assessed the effectiveness of using an online remote digital lab in teaching advanced digital design concepts with a suggested template for properly evaluating remote laboratories. The impact of using PBL approaches to enhance teaching Digital Logic Design has been assessed in several studies, including [29–31] with the main focus on evaluating the overall impact of the proposed approaches on students' performance. Compared to these studies, the main focus of this work is to assess the impact of PBL on students with different performance levels.

3. Course Overview

The Digital Logic Design (22241) course taught at Princess Sumaya University for Technology (PSUT) is a mandatory second-year course for five programs in the School of Engineering; Computer Engineering, Network and Information Security Engineering, Communications Engineering, Electrical Power and Energy Engineering, and Electronics Engineering. The course is also mandatory for two programs in the School of Computing Sciences; Computer Science, and Software Engineering, and elective for the Computer Graphics and Animation program.

The course content is generally divided into combinational and sequential logic. The combinational logic part covers the basics of digital logic design, including numbering systems, Boolean algebra, K-maps, combinational circuits analysis and design, and standard building blocks such as adders/subtractors, comparators, decoders, and multiplexers. The sequential logic part, which is the focus of this work, starts by introducing the basic storage elements such as latches and flip-flops. Then it discusses the analysis and design of sequential logic circuits. The analysis part focuses on describing the functionality of given sequential circuits as state transition tables and diagrams. On the other hand, the design part aims to provide students with the necessary background and techniques to build sequential circuits that perform specific functionalities described as finite state machines (FSMs) or descriptive problem statements. Some special sequential circuits, including registers and counters, are discussed at the end of the sequential logic part.

According to the continuous improvement process conducted and maintained by the department of Computer Engineering (CE) at PSUT, each course must have a set of well-specified measurable Course Learning Outcomes (CLOs). These outcomes can be mapped to the Student Outcomes (SOs) of the national and international accreditation of the Computer Engineering program and other programs that need some service courses from the CE department. The Digital Logic Design course has the following five CLOs that are measured using typical assessment tools, including exams, quizzes, and assignments:

(1) Understand numbering systems and codes.
(2) Learn the fundamental hardware components used in digital systems.

(3) Design combinational logic circuits for specific design requirements.
(4) Design sequential logic circuits for specific design requirements.
(5) Understand basic memory operations.

The Digital Logic Design course is considered the first core course for Computer Engineering students. Digital systems are becoming increasingly involved in almost every system, and students are expected to deal with such systems during their studies. Hence, this course is also of critical importance for other programs. The course is a prerequisite of several laboratories and courses in the curriculum of all the aforementioned engineering and computing sciences programs, including Digital Logic Laboratory, Computer Organization and Assembly Language, Microprocessor Systems, Computer Architecture, and Embedded Systems.

4. Methodology

This section presents the pedagogical challenges, the project description, the study participant, and the evaluation criteria involved in the proposed project-based learning approach.

4.1 Pedagogical Challenges

In this subsection, the pedagogical challenges that need to be addressed and taken into consideration when designing the proposed project are investigated.

4.1.1 The First Design Experience

The proposed project can be divided into three phases; design, implementation, and testing. The design phase is based on students' understanding of the theoretical material and examples discussed in class. Designing sequential circuits is more challenging for students than analysis of existing circuits. The analysis is based on systematic step-by-step procedures a student can follow to describe the circuit's functionality as a state table and state diagram. On the other hand, the design relies on understanding the problem statement and formulating it as a state diagram before proceeding with the systematic design procedures. The implementation and testing phases are conducted using the software simulator. In addition to the online tutorials provided to students, the course instructors gave a short tutorial on building and simulating one of the design problems discussed in class.

4.1.2 Focus Efforts on Concepts not the Tool

Choosing a software simulator for PBL in this course is not an easy task since it is the first experience for students to build, simulate, and test a digital circuit. It is more feasible to choose an easy-to-learn simulator so that students can focus on understanding how the circuit works without spending a lot of time learning how to run and configure the simulator. Consequently, the chosen simulator should be schematic-based with an easy-to-use Graphical User Interface (GUI). More senior computer engineering classes and labs, like digital logic lab, computer architecture I & II, and computer design lab, provide students with the opportunity to learn and use Hardware Description Language (HDL)-based simulators and development kits. Among the several available schematic-based software simulators, including those described in [32], Logisim simulator [33] is used in the PBL approach proposed in this paper. The reasons behind selecting this simulator were that it is free, and easy to use.

4.1.3 Combinational Vs Sequential Timing

As discussed in Section 1, one of the most critical challenges in the sequential logic part is its new timing concepts and strategies. To help students understand these new concepts easily, the used simulator supports both manual and automatic changing of the clock signal that controls the timing of all events in synchronous sequential circuits, including the problem to be designed and implemented in the proposed project. In the early stages of the project, students can focus on basic timing concepts, such as edge-triggered operations, by generating positive/negative edges of the clock manually so that they have enough time to watch the changes in the circuit state and outputs. Automatic changing of the clock, on the other hand, is very helpful in relating clock frequency to the overall speed of the circuit. For instance, students can control the speed of a counter that counts a given sequence of numbers on a seven-segment display by changing the frequency of the input clock signal.

4.1.4 Maintaining Academic Integrity

Given the large number of students in this multi-section and multi-instructor course, ensuring academic integrity and honesty during the course of the project is challenging. In addition to the announcement of university rules and regulations related to academic integrity and honesty, a personalized assessment approach [34] is adopted in the proposed project to ensure academic integrity and honesty. More details on the adopted approach are presented later in this section.

4.2 Project Description

Students are required to design a simple digital system that is composed of a combinational logic

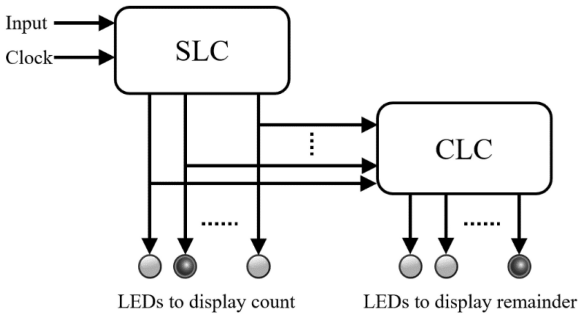


Fig. 1. Block diagram of the digital circuit to be implemented in the project.

circuit (CLC) and a synchronous sequential logic circuit (SLC), as shown in Fig. 1.

The SLC is a counter, built using JK flip-flops, that behaves based on an external input. The count value should be displayed on Light Emitting Diodes (LEDs) and is also the input to the CLC component. The behavior of the counter to be designed depends on the least significant digits of students' university ID, specifically, the ones and tens digits. Table 1 lists the behavior of the counter to be designed based on these two digits. The CLC is supposed to calculate the remainder of dividing the count value by some value R and display the result on LEDs. The value R is either the ones digit in the student ID if it is between 2 and 5, or the student's section number otherwise.

The simulation environment – for one of the submitted projects – is shown in Fig. 2. Students can either run the clock manually or automatically, at a specific frequency of their choice, using the Simulate Menu. The proposed PBL approach has

Table 1. Counter behavior based on the first two digits of student ID

Student ID		**Counter Number**	**External Input**	**Counter Behavior**
Tens Digit	**Ones Digit**			
Even	Even	I	0	0, 3, 2, 6, 4, 1, 5, 7, 0, 3, 2, 6, 4, 1, 5, 7, ...
			1	Counter pauses at the current count
Even	Odd	II	0	0, 5, 2, 4, 6, 1, 3, 7, 0, 5, 2, 4, 6, 1, 3, 7, ...
			1	0, 7, 3, 1, 6, 4, 2, 5, 0, 7, 3, 1, 6, 4, 2, 5, ...
Odd	Even	III	0	Counter pauses at the current count
			1	0, 7, 5, 1, 4, 6, 2, 3, 0, 7, 5, 1, 4, 6, 2, 3, ...
Odd	Odd	IV	0	0, 2, 4, 6, 7, 5, 3, 1, 0, 2, 4, 6, 7, 5, 3, 1, ...
			1	0, 1, 3, 5, 7, 6, 4, 2, 0, 1, 3, 5, 7, 6, 4, 2, ...

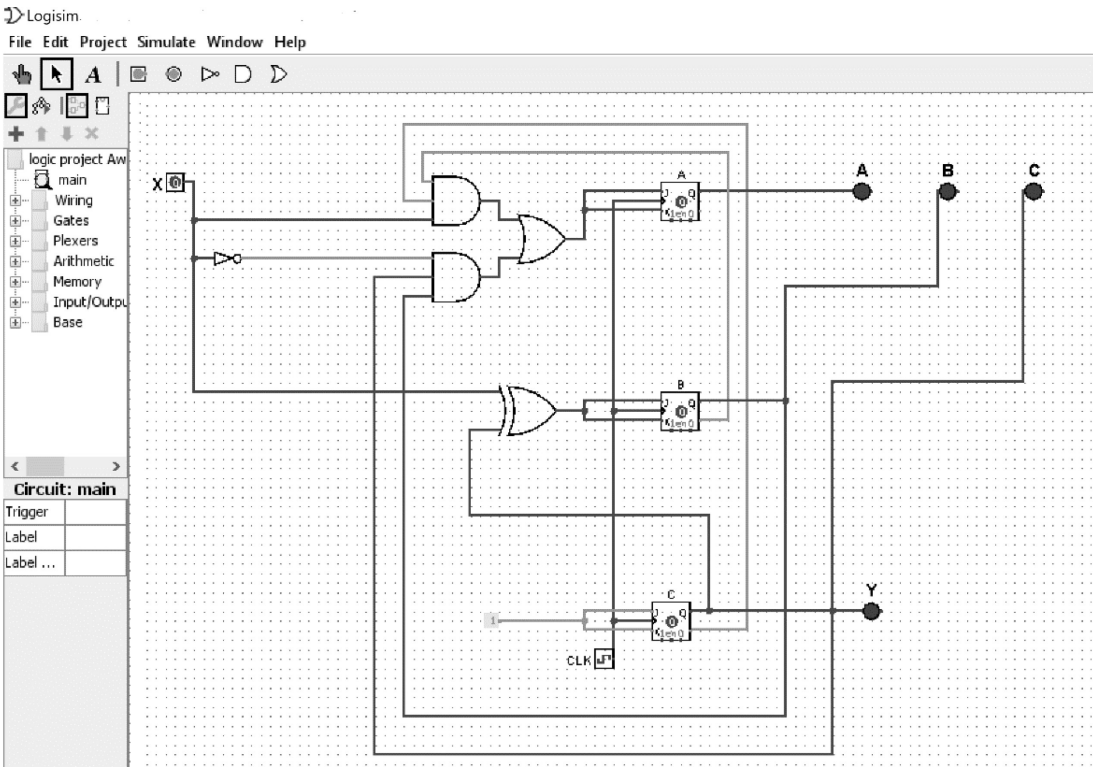


Fig. 2. The simulation environment used in the proposed PBL approach.

been applied to another semester, as shown in Table 2 using a similar design problem with different count sequences and a personalized assessment approach based on a random number generator.

According to the definitions of PBL and PjBL presented in Section 1, the design project described in this subsection falls under the umbrella of PBL.

4.3 Study Participants

The results presented and analyzed in this paper are based on applying the proposed PBL for the classes offered in the Spring 2020 and Spring 2021 semesters in comparison with the four previous semesters without a project, as shown in Table 2. The table shows that the no project group was 326 students, and the *With Project* was 261 students. It is worth mentioning that the semesters without a project were selected so that at least one of the authors is an instructor of the course in the selected semester, and the total number of students is close to the number of students in the two semesters with a project. The differences between these two groups are shown to be statistically significant, as discussed in the following section.

4.4 Evaluation Criteria

Students are required to work individually on the project described in the previous subsection. The course instructors assessed the submitted work according to the rubric described in Table 3.

The proposed approach relies on assessing the impact of PBL on students with different performance levels. Accordingly, a baseline performance measure must be specified to determine each participant's performance level. In this work, students' performance in the introductory part of the course is used for this purpose, as discussed in the following section.

Table 2. Distribution of Students on Different Semesters

Semester	No of Students	Project Status
Spring 2015	76	No Project
Fall 2015	97	No Project
Spring 2016	65	No Project
Fall 2018	88	No Project
Spring 2020	176	With project
Spring 2021	85	With project

Table 3. The Evaluation Rubric

Phase	Criteria	Max. Grade %
Sequential Logic Design (40%)	State Diagram/Table	10%
	Flip Flop Inputs (Excitation Tables)	10%
	Simplified Input Equations (K-Map)	20%
Combinational Logic Design (30%)	Truth Table	15%
	Simplified Output Equations (K-Map)	15%
Simulation using Logisim (30%)	Circuit Implementation in Logisim	15%
	Working Simulation	15%

5. Results

This section discusses the results of administering the project and its impact on students. First, an overall discussion is presented in subsection 5.1. Then in subsection 5.2, the project's impact on different student groups is presented. Finally, subsection 5.3 presents the project's impact on individual students' performance. Results reported and discussed in this section are based on the overall distribution of participants by their project status after applying the proposed PBL approach, as shown in Fig. 3.

5.1 Overall Project Impact Analysis

To compare the project's impact on the student's performance, one would need to compare the students' levels at the beginning of the semester. This will be referred to as the baseline for the students. To create the baseline performance, the student's score in the first couple of quizzes in the class was used. These two quizzes are fundamental and can be used as a baseline benchmark. Fig. 4 shows that the baseline for the No Project students (6.1) was higher than that of the *With Project* (5.3). This can be interpreted to indicate that we are starting with a slightly weaker group of students in the case of *With Project*. The two-tail t-test value was calculated to be: 0.000324, indicating both groups are not identical. The error bars shown in this figure and the remaining figures are the standard deviations of the grades, where the upper and lower bars represent one standard deviation above and below the average grades, respectively.

Fig. 5 shows the difference in the achievement in both the sequential analysis and the sequential

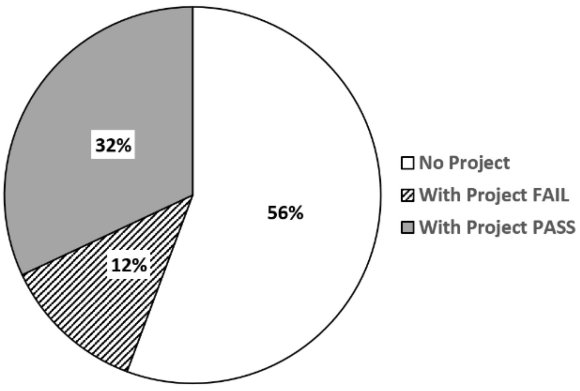


Fig. 3. The breakdown of Students by their project Status.

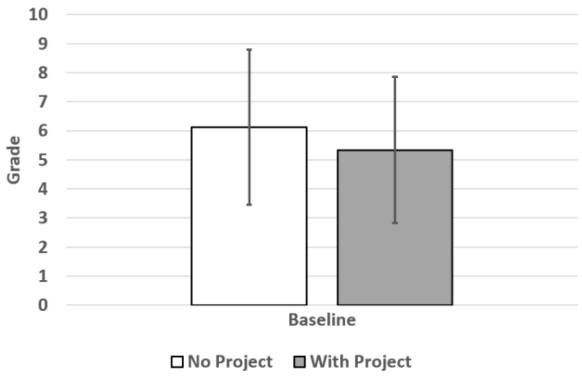


Fig. 4. Baseline Comparison Per Project Status.

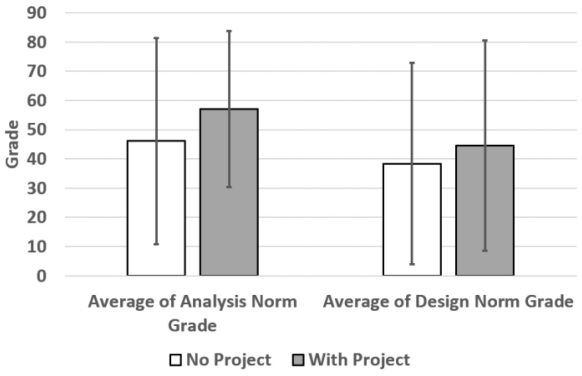


Fig. 5. Average Performance of Students in Sequential Circuits in the Final Exam Per Project Status

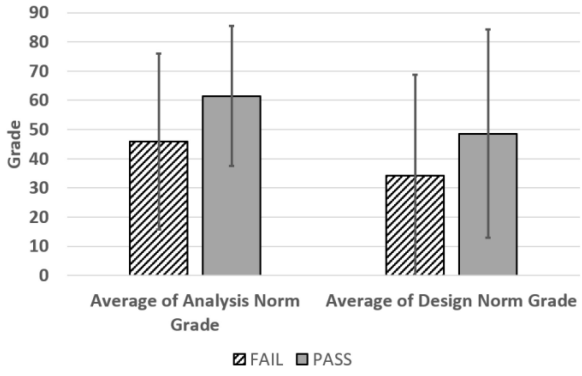


Fig. 6. Average Performance of Students in Sequential Circuits in the final Exam Per Project Completion.

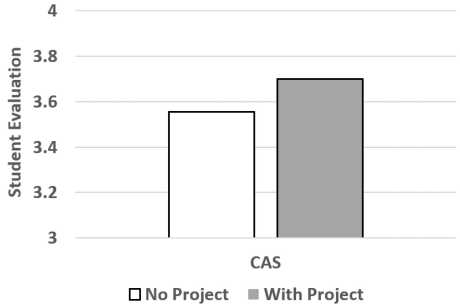


Fig. 7. Course Assessment by the Student Per Project Status.

design of both groups: *No Project* and *With Project*. The shown results are their average normalized grades in the final exam. It can be clearly seen that students in the *With Project* achieved better than the *No project.* Scoring {*No Project*: 46.1%, *With Project*: 57.1%} on average in the analysis of the sequential circuits. Meanwhile, in the design of sequential circuits, the gap was smaller, with averages being {*No Project*: 38.4%, *With Project*: 44.6%}. The one-tail t-test value was calculated to be 1.8328 E-05 for the analysis normalized grades and 0.01815 for the design normalized grade. This emphasizes confidence in the aforementioned results.

It was also worth assessing the difference between passing the project (i.e., scoring more than or equal to 50%) versus failing it for those students who have taken the project. Fig. 6 shows the normalized average score for the analysis and design of sequential circuit questions in the final exam. Here it can be seen that those who passed the project scored better than those who failed. The scores were {Pass: 61.5%, Fail: 45.8%} for the analysis part, and {Pass: 45.6%, Fail: 34.3%} for the design. It is clear that the design part results have been consistently worse than those of the analysis, as it requires deeper knowledge and more skills. However, based on the results presented so far, one can't conclude that the project was the reason behind this performance enhancement. The one-tail t-test value was calculated to be 8.873 E-06 for the analysis normalized grades and 0.001952 for the design normalized grade. This emphasizes confidence in the aforementioned results.

In addition to assessing the performance comparison from the instructor's perspective, a student perspective was also considered. At the end of each semester, students are asked to fill in an anonymous survey for the Accreditation Board for Engineering and Technology (ABET) for certain classes. In this survey, students rate how well they comprehended/achieved certain outcomes, from one being the lowest to five being the highest, how well they think they comprehended/achieved certain outcomes. One of these outcomes in the digital design class is sequential circuit design. Fig. 7 shows that the *With Project* group has evaluated the outcome slightly higher than the *No Project* group. This is a valuable result as this confirms the finding that the *With Project* group has a better understanding of the topic than the *No Project*.

5.2 Analysis of Performance Impact per Group

To be able to assess the project's impact on different student groups, the baseline described earlier was used to split the students into three different groups {High, Medium, Low} in terms of their academic

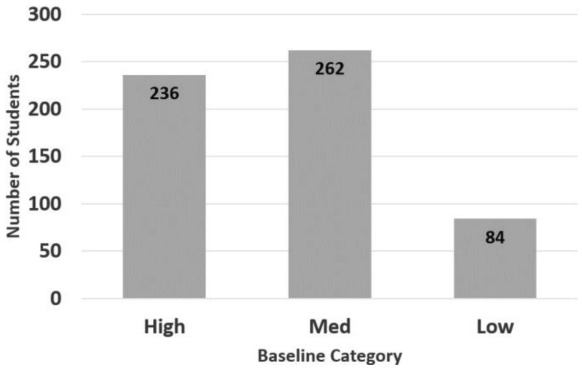


Fig. 8. The breakdown of Students by their Baseline Category.

performance, as shown by Equation 1. Fig. 8 shows the distribution of all students by their corresponding group. It can be seen that there are 84 Low performing students, 262 Medium, and 236 High performing students.

$$Student\ Level = \begin{cases} Low, & 3 > \text{grade} \geq 0 \\ Medium, & 7 > \text{grade} \geq 3 \\ High, & 10 \geq \text{grade} \geq 7 \end{cases} \quad (1)$$

Figs. 9 and 10 show the project's impact on the students using two measures. Fig. 9 focuses on the normalized grades of the sequential design part in the final exam. In contrast, Fig. 10, tackles their scores in the entire final exam.

In Fig. 9a, it can be seen that students *With Project* have consistently outperformed the No Project students with the most significant difference is shown in the Low group of students {*With Project*: 38.0%, *No Project*: 24.6%}. The difference was less significant in the High and Medium groups. Meanwhile, Fig. 9b shows the difference between those who passed the project and those who failed. Here it can be seen that passing the project had minimal impact on High performing students but a significant on the Medium group. The difference in scores was significant: {Pass: 43.6%, Fail: 26.7%}.

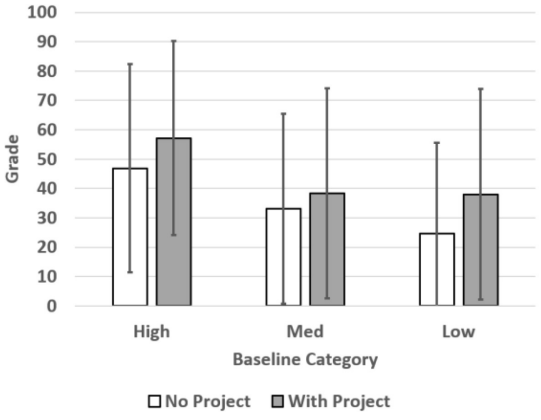
The other measure used to assess the group level performance was the entire final exam grades. Fig. 10a again shows that the *With Project* students have performed better than the *No Project* students across all performance level groups. Again, the Low group achieved the most prominent performance gap: {*With Project*: 16.7%, *No Project*: 10.7%}. Here the one-tail t-test values were calculated to be: {High: 0.001448, Med: 0.002831, Low: 0.000212} for the final exam grades broken between the *With Project* and *No Project* grades, all values are well below the 5% limit.

Similarly, Fig. 10b shows the final exam average score difference between those who passed the project and those who failed it. It can be noted that across all students' performance levels, those who passed the project scored better than those who failed it. Here the one-tail t-test values were also calculated to be: {High: 0.024406, Med:0.014823, Low: 0.005853} for the final exam grades broken between the Pass and Fail grades, all values are well below the 5% limit. It can be noted by examining Fig. 9a and Fig. 10a that the Low performing group is the one group that benefited the most from the project.

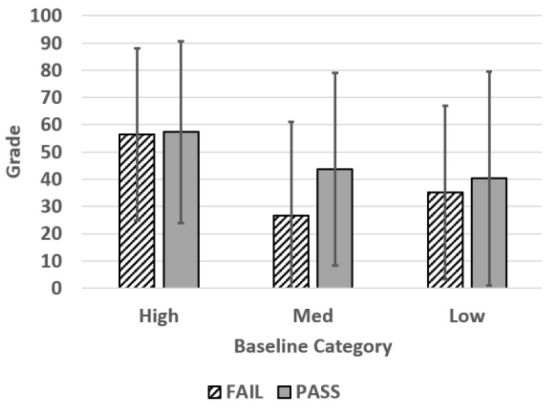
5.3 Individual Students' Performance Impact Analysis

The results of the previous section eliminated the doubt that the relation between the students' performance and the project is mere correlation and not causation. Because had it been a correlation, the impact would not have been visible across all student performance levels.

To further verify the project impact, the individual student performance level was assessed again at the end of the semester (Final rating). The final

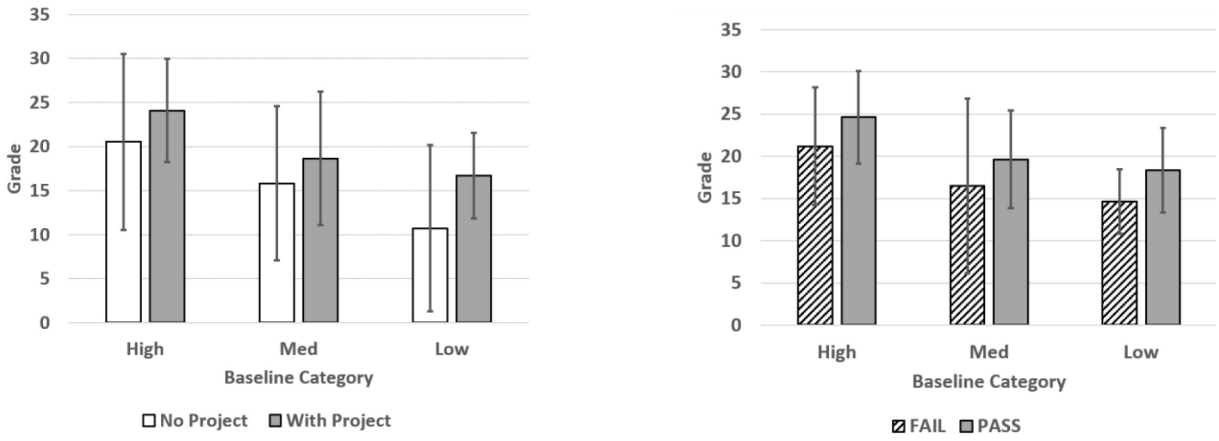


(a) Project Status



(b) Project Completion

Fig. 9. Design Normalized Grades Per Project.



(a) Project Status (b) Project Completion

Fig. 10. Final Exam Grades Per Project.

rating of the performance level was captured using the total grade the student achieved in the course and the following Equation 2:

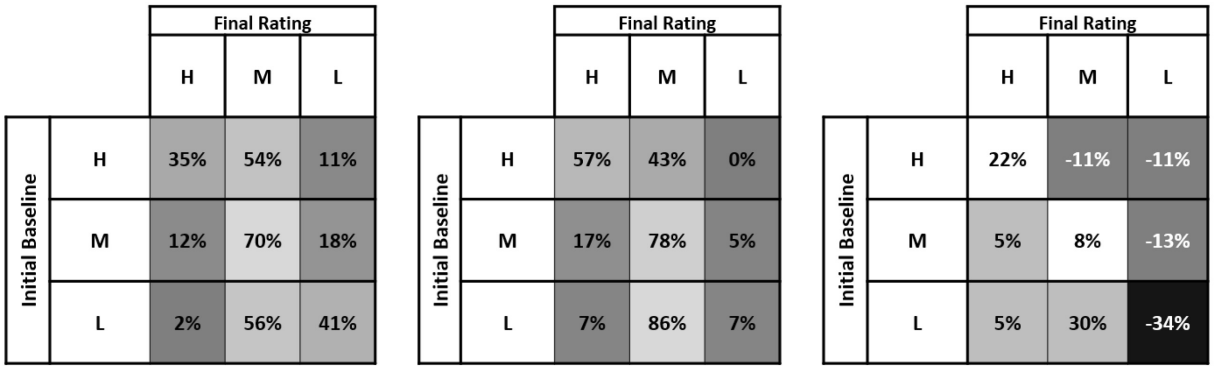
$$Student\ Level = \begin{cases} Low, & 30 > \text{grade} \geq 0 \\ Medium, & 70 > \text{grade} \geq 30 \\ High, & 100 \geq \text{grade} \geq 70 \end{cases} \quad (2)$$

The rows in Fig. 11 show the initial baseline at the beginning of the semester, while the columns show the Final rating. The row percentages add to 100%, which is the initial baseline population per class. So, in Fig. 11a, it can be seen that 35% of the high-performing students maintained their rating, while 54% dropped to a Medium rating, and 11% dropped from High to Low.

Ideally, in this figure, one would want to maximize the percentage of students that improved their rating, shown in the lower left triangle {M-H, L-H, L-M}. This is in addition, to maximizing the High or Medium students who maintained their rating {H-H, M-M}. At the same time, one would want to minimize the percentage of students whose performance got worse, shown in the upper right triangle {H-M, H-L, M-L}. In addition to minimizing the Low performing students who could not improve their rating as stayed as Low {L-L}.

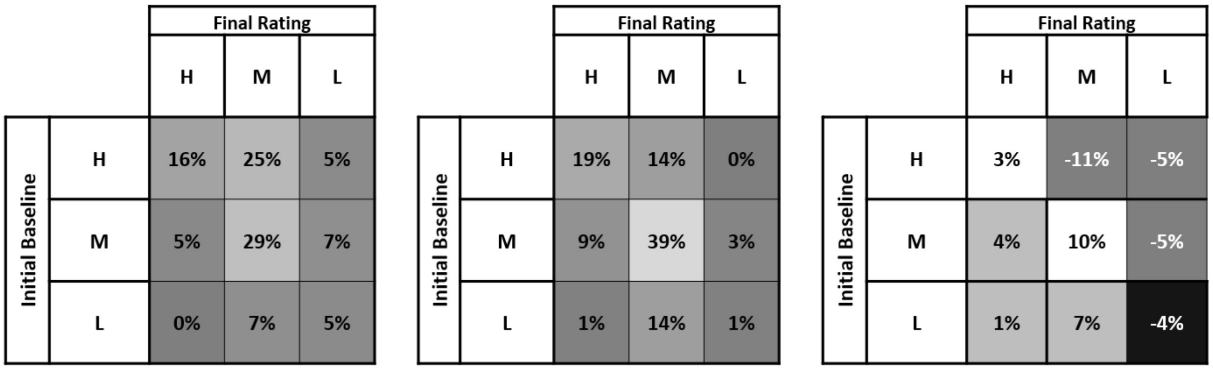
Fig. 11a shows the breakdown for the *No Project* students, while Fig. 11b shows the breakdown for the *With Project* Students. To be able to see the project's impact on the students, Fig. 11c shows the difference in the percentages between (a) and (b). It shows a positive difference in the lower left triangle, where the student performance has improved. For example, the percentage of students who started as Low and ended up as Medium has increased by 30%. Similarly, the {H-H: 22%, M-M:8%} indicated that High and Medium performing students who maintained their ratings have positively increased.

On the other hand, when considering the groups whose performance got worse – the upper right triangle – it can be seen that all percentages are negative. For example, students with medium baseline and Low final ratings have dropped by 13%. This means that the number of students whose performance has worsened has decreased. In addi-



(a) No Project (b) With Project (c) Difference between a & b

Fig. 11. Performance Change of Students Per the Baseline Class.



(a) No Project (b) With Project (c) Difference between a & b

Fig. 12. Performance Change of Students Per All Classes.

tion, Low-performing students who remained in the category decreased by 34%.

Fig. 12 shows similar results to that shown in Fig. 11. However, here they are normalized by the total of all classes instead of being normalized per baseline class. Thus, the entire matrix would add to 100% in Fig. 12a and Fig. 12b. Results in Fig. 12c support the same conclusion, that the number of students has increased in all desirable categories and decreased in all unfavorable ones.

6. Discussion

The multi-level assessment methodology used in the previous section consistently shows the positive impact of the proposed problem-based learning approach across all performance groups. Students who had a project performed better than those who didn't have a project. Assessment results also show that students who had a project and passed it performed better than those who failed it. The standard deviation error bars, reported along with the average scores in the previous section, are very important to show how spread the students' grades are around the average scores. It is clear from the reported error bars that the grades are widely spread. Hence, it is of great importance to consider a student-level assessment methodology and look at the impact of the proposed approach on different groups of students, not just the whole group of students represented by a single average score. Although standard deviation is not a statistical test by itself, the overlapped reported values highlight the need to use statistical tests, including the t-test used in this work, to assess the significance of the differences between the reported average scores and show that they are not due to chance or sampling errors.

In addition to the quantitative assessment results reported in this study, it is worth highlighting some qualitative feedback from the instructors' perspective. The simulation-based task used in the proposed approach motivated many students to simulate some of the sequential circuits discussed in class, including basic flip flops, counters and shift registers. The impact of the proposed approach on average students has been recognized by the critical questions and discussions they raised during classes and office hours, that are typically raised by high-performance students. Moreover, the proposed approach made it feasible for the instructors to discuss some advanced topics that were usually difficult to discuss toward the end of the course due to time limitations. One such example is the topic of the Unused States in Finite State Machines. The instructors were comfortable discussing this topic with a minimum time by asking students, who became familiar with the simulation software, to simulate a counter with some unused states and analyze its behavior.

The results reported in this work have to be understood in light of the following limitations that we acknowledge. First, we were not able to use a more complex problem than the one used in this study due to the fact that the background material required to complete the proposed task is discussed toward the end of the semester, which is typically a very busy period for students. Additionally, the proposed baseline metric does not include any performance measures from pre-requisite courses, which would make the baseline benchmark more robust, since the course under study is an introductory course with no pre-requisite. Finally, we acknowledge the lack of documentation of qualitative feedback from students as we relied on an independent quantitative student survey, conducted by the quality assurance unit, to assess the impact of the proposed approach from students' perspective.

7. Conclusion

In this paper, a problem-based learning approach

has been proposed to improve students' performance in sequential logic design, the most challenging part of a typical digital logic design course. The project-oriented problem has been developed based on investigating the pedagogical approach and methodologies needed for the most effective implementation and assessment. The systematic student-level analysis of the evaluation results shows that the project enhanced the students' performance from all academic levels. In fact, more students have improved their performance level from a lower to a higher category, and less percentage dropped to a lower-performing group. As a next step, we intend to investigate other pedagogical approach, including pedagogical differentiation, that provide instructors with the flexibility to factor in the variations in students' performance levels in the project's design. This is expected to cater more to the needs of each group and positively impact their academic performance.

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Awos Kanan is Assistant professor in Computer Engineering at Princess Sumaya University for Technology, Amman, Jordan, and Adjunct Professor at the University of Victoria, Victoria BC, Canada. Received his PhD degree from the University of Victoria, Canada, MSc and BSc degrees from Jordan University of Science and Technology, Jordan, all in Computer Engineering. Dr. Kanan has more than 15 years of academic experience in Jordan, Saudi Arabia and Canada. His research interests are in Data Mining, Parallel Computing, Hardware Acceleration for Big Data processing, Applied Machine Learning, Meta-Heuristic Optimization Algorithms, and Computer Networks. He is a member of IEEE and Jordanian Engineers Association (JEA).

Rajaa Alqudah received her BS degree in computer engineering from Yarmouk University, Jordan, in 2003, her MSc degree in computer engineering from The Northeastern University, USA in 2007, and her PhD degree in computer engineering from Syracuse University, USA in 2011. She currently serves as an assistant professor of Computer Engineering at Princess Sumaya University for Technology (PSUT), Jordan. Rajaa has more than 9 years of industry experience at Intel Corporation working in pre-silicon validation.

Amjed Al-Mousa, a senior IEEE member, and an associate professor of computer engineering at PSUT since 2012. Dr. Al-Mousa has received his PhD from Santa Clara University, MSc from Virginia Tech, and BSc from the University of Jordan all in Electrical Engineering. Dr. Al-Mousa combines this academic experience with more than 13 years of industry experience at Silicon Valley. He started his career by working at Intel Corporation in 2001 and later moved to PDF solutions, to work on Design for Manufacturing software tools. After that, he assumed a senior manager position for data analytics at SEVEN networks. Dr. Al-Mousa has served twice as the head of the computer engineering department at PSUT. He developed course content in the fields of Artificial Intelligence, Machine Learning, Cloud Computing and Big Data. His research interests are in the fields of intelligent systems design and machine learning with varying industrial applications.